5-Bit, Ka-Band Core Chip
34 - 36 GHz

CGY2350UH/C1
Rev. V1

Features

- Gain: 4 dB (Rx), 3 dB (Tx)
- Noise Figure: 6 dB (Rx)
- RMS Phase Error: 5°
- RMS Amplitude Error: 0.4 dB (Tx), 0.6 dB (Rx)
- Output P1dB: 10 dBm (Tx)
- Input Return Loss: -11 dB (Rx), -13 dB (Tx)
- Output Return Loss: -13 dB (Rx), -8 dB (Tx)
- Total Power Consumption: 250 mW @ 3.3 V
- Chip Size: 3000 x 4700 µm
- Tested, Inspected Known Good Die (KGD)
- RoHS* Compliant

Applications

- Radar, Antennas
- Telecommunication
- Instrumentation

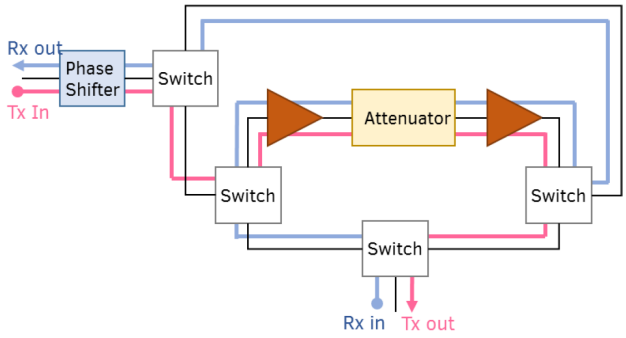
Description

The CGY2350UH/C1 is a high performance pHEMT technology GaAs MMIC 5-bit core chip operating in Ka-band. It exhibits 2 RF ports including 2 switches. It includes a 5-bit digital phase shifter, a 5-bit digital attenuator, and switches. It has a phase shifting range of 348° and a gain setting range of 15.5 dB. It covers the frequency range from 34 to 36 GHz.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

This die is manufactured using 0.18 µm gate length ED02AH pHEMT Technology. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2350UH/C1	On wafer measured die
CGY2350UH/C1/EK	Evaluation Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 34 - 36 GHz, V_{DN} = +5 V, V_{SN} = -5 V, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	Rx Mode Tx Moe	dB	3.0 2.0	4.0 3.0	4.8 4.0
Gain Variation	—	dB/°C	—	—	0.065
Input Return Loss	Rx Mode Tx Mode	dB	—	—	-11 -13
Output Return Loss	Rx Mode Tx Mode	dB	—	—	-13 -8
Phase Shift Range	—	°	—	348.75	—
Phase Shift Step	—	°	—	11.25	—
RMS Phase Shift Error	Rx Mode Tx Mode	°	—	—	5 5
Attenuation Range	—	dB	—	15.5	—
Attenuation Step	—	dB	—	0.5	—
RMS Attenuation Error	Rx Mode Tx Mode	dB	—	0.2 0.5	0.4 0.6
Noise Figure	—	dB	—	5	6
Power Consumption	Rx Mode Tx Mode	mW	—	180 205	—
Input P1dB	Tx Mode	dBm	10.0	11.5	12.0

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Control I/O Pins Voltage VDN VSN	 0 V to +3.3 V -3.0 V to 0 V
Positive Supply Voltage Rx & Tx	 0 V to +3.3 V
Negative Supply Voltage Rx & Tx	 -5 V to 0 V
Total Drain Current Rx Mode Tx Mode	 0 to 53 ma 0 to 45 mA
Input Power	0 dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

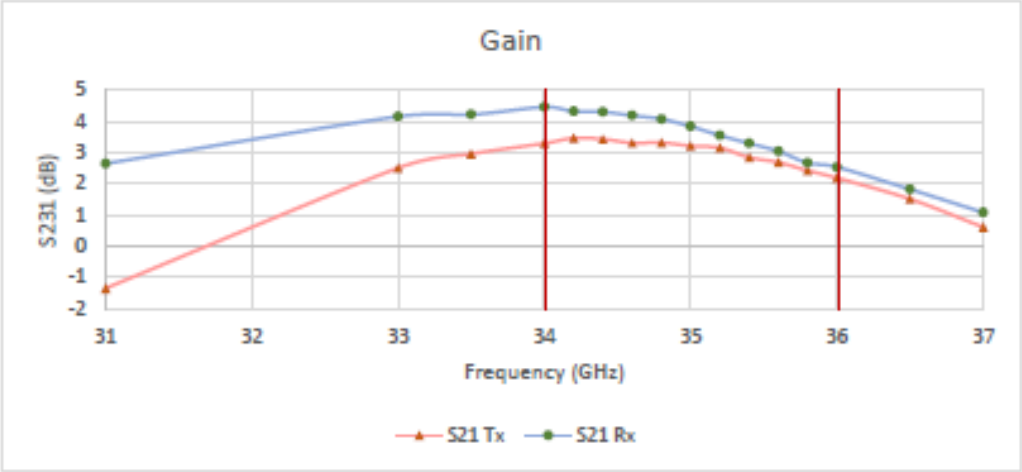
Handling Procedures

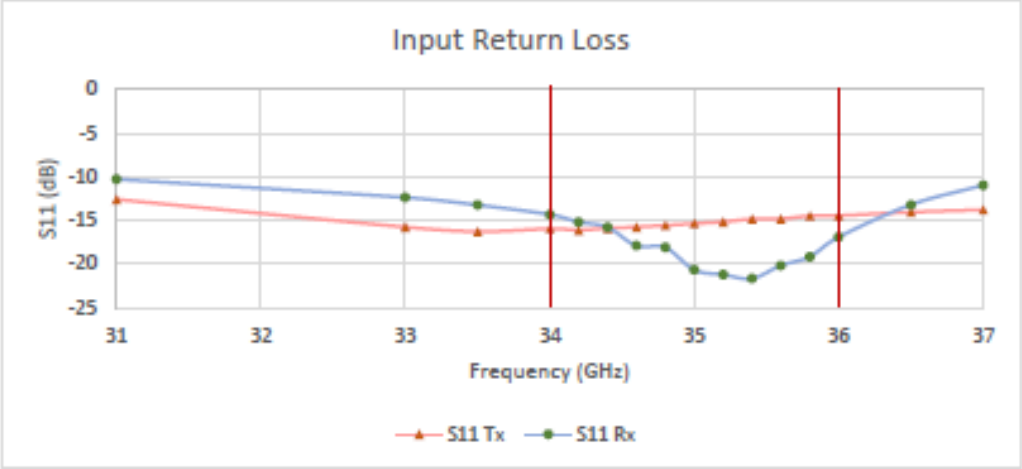
Please observe the following precautions to avoid damage:

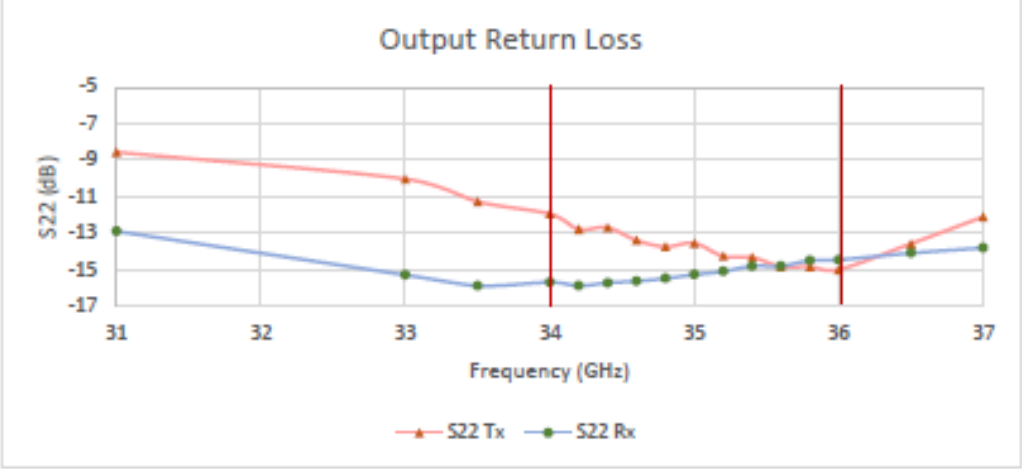
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

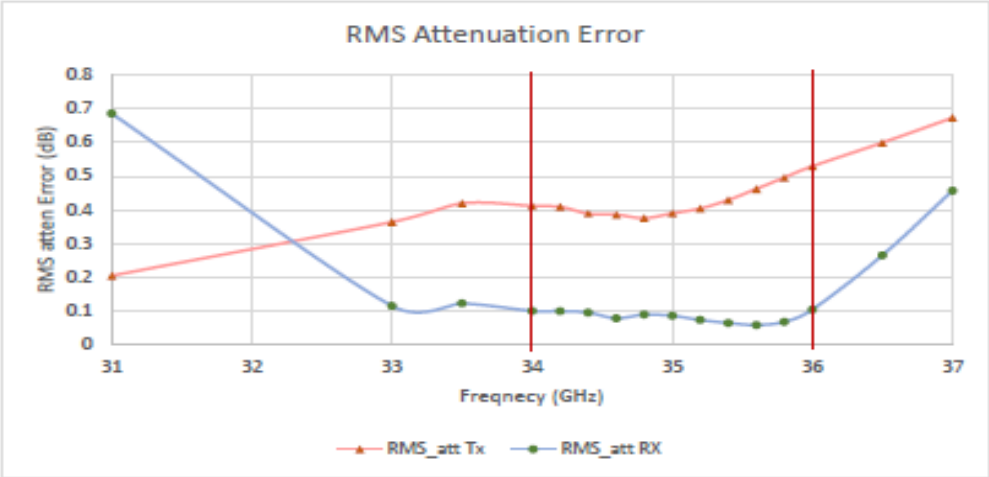
Typical Performance Curves: On Wafer Measurements

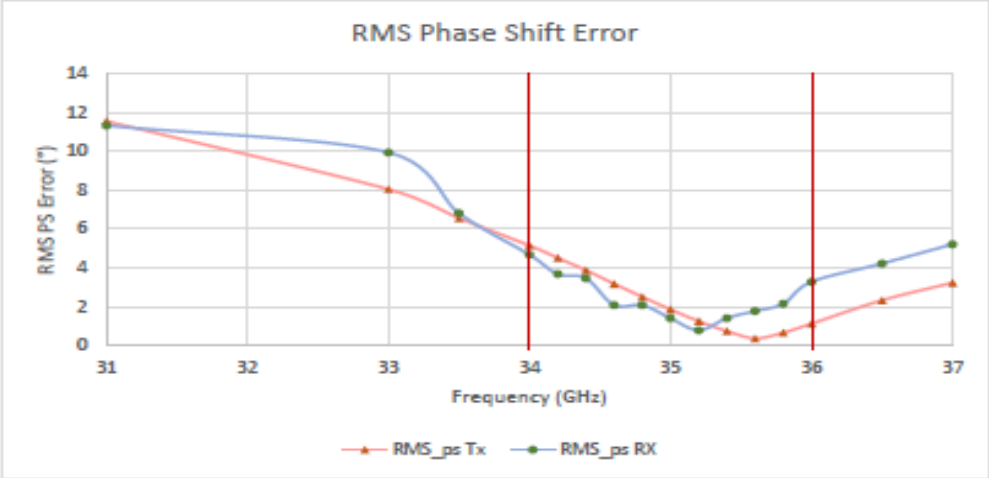






Typical Performance Curves: On Wafer Measurements





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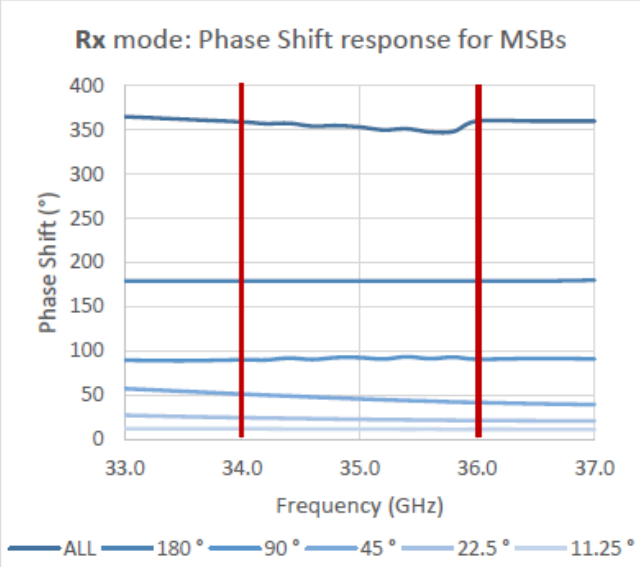
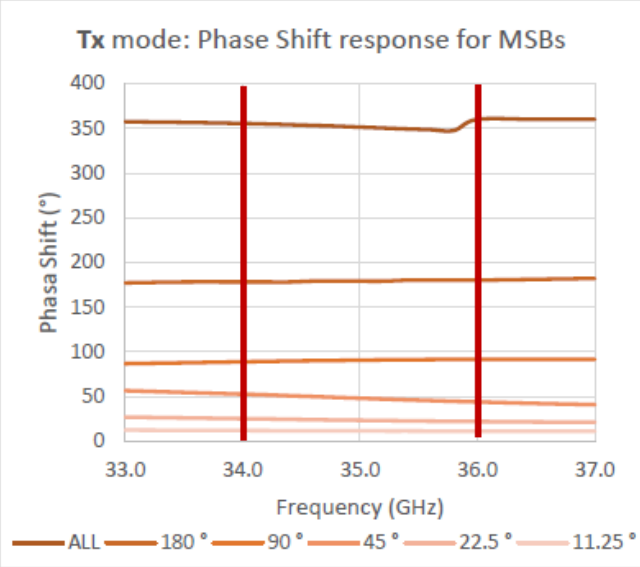
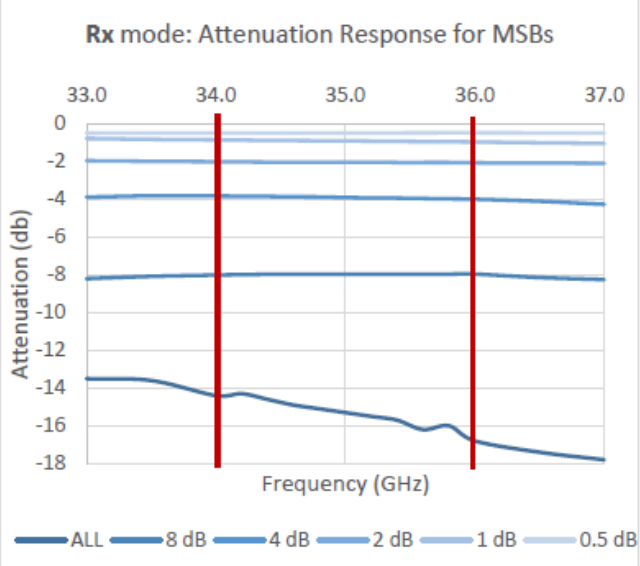
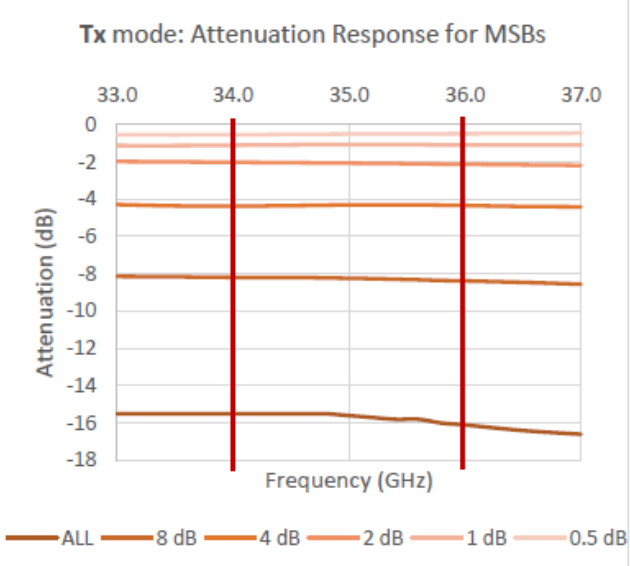




Attenuator response





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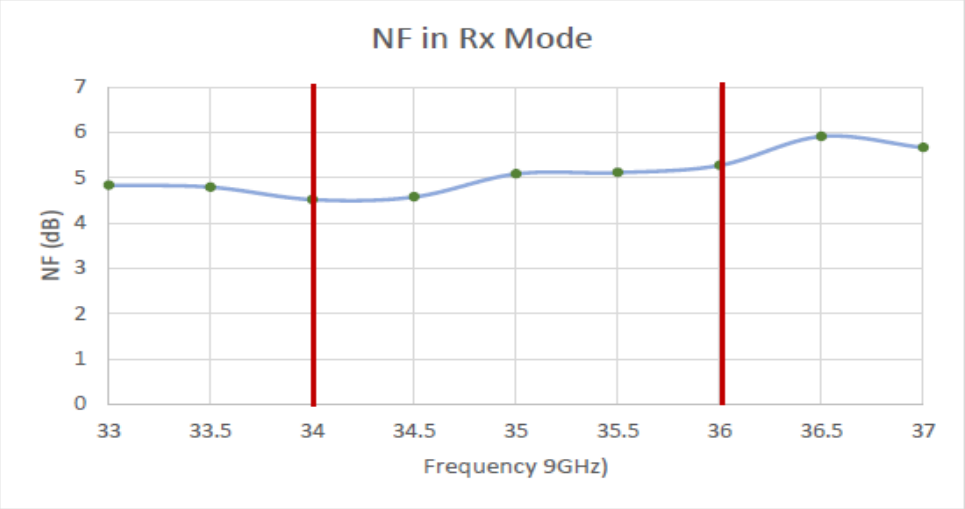
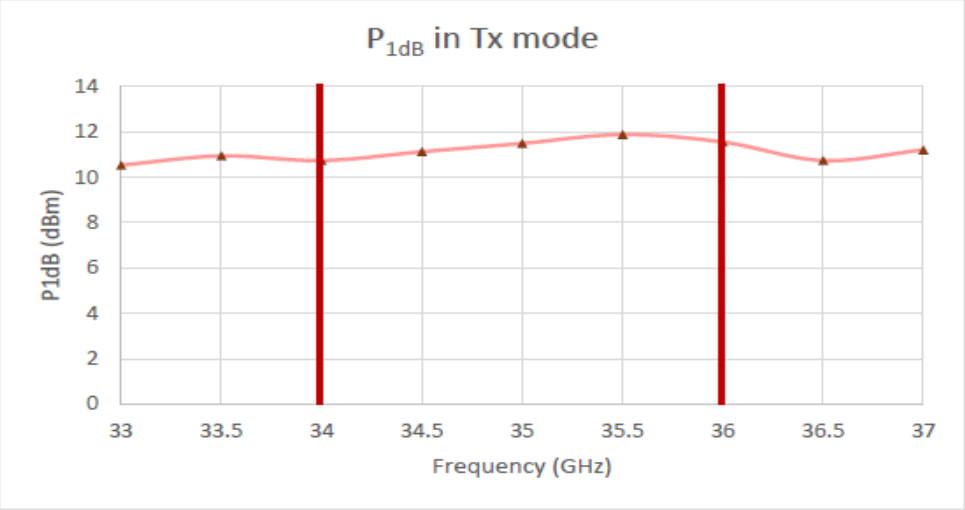




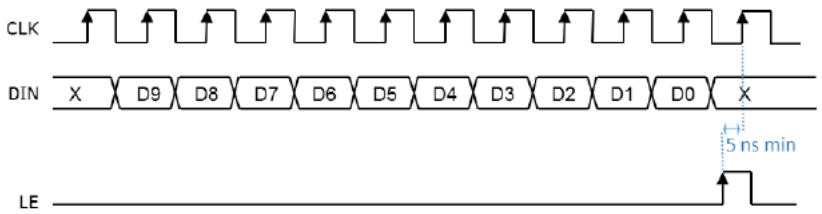
Data (Reference State LOW)

Bit #	Description	Theoretical Value
B0	Phase State Control	11.25°
B1		22.5°
B2		45°
B3		90°
B4		180°
B5	Attenuation State Control	0.5 dB
B6		1 dB
B7		2 dB
B8		4 dB
B9		8 dB

Control Voltage (CMOS Standard Logic)

State	V Min.	V max.
Low	0 V	1 V
High	2.5 V	V_{DN}

Timing Diagram



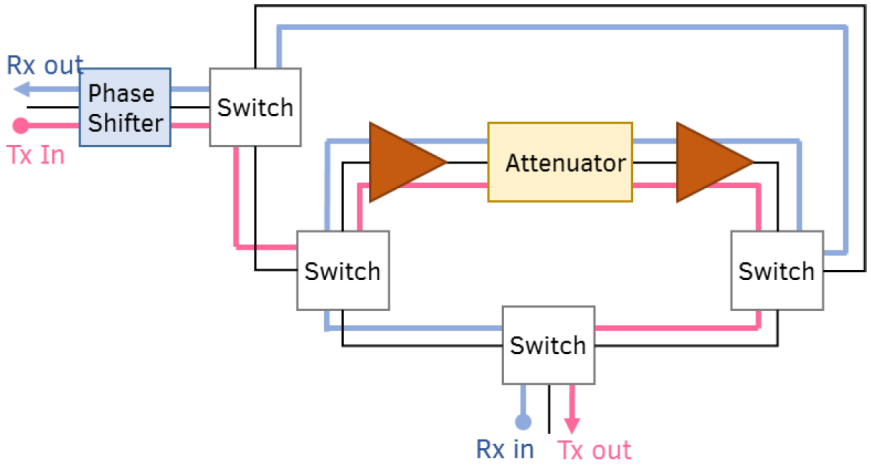
Data In (DIN) is sampled at the rising edge of the Clock (CLK) signal. First loaded bit is D9 (8 dB Attenuation).

Rising edge of Latch Enable (LE) must occur after all 10 bits are loaded.
Data In is transferred to the operating register (and Attenuator/Phase Shifter settings are changed) on the rising edge of Latch Enable.

The Clock (CLK signal) defines the speed of changing Attenuator/Phase Shift setting, the setting could be changed in 600 ns (if 20 MHz Clock) or 54 ns (if 240 MHz Clock).

Setup and hold times should be greater than **5 ns**:
-For DI and LEI with respect to CI rising edge
-For LEI with respect to CI falling edge

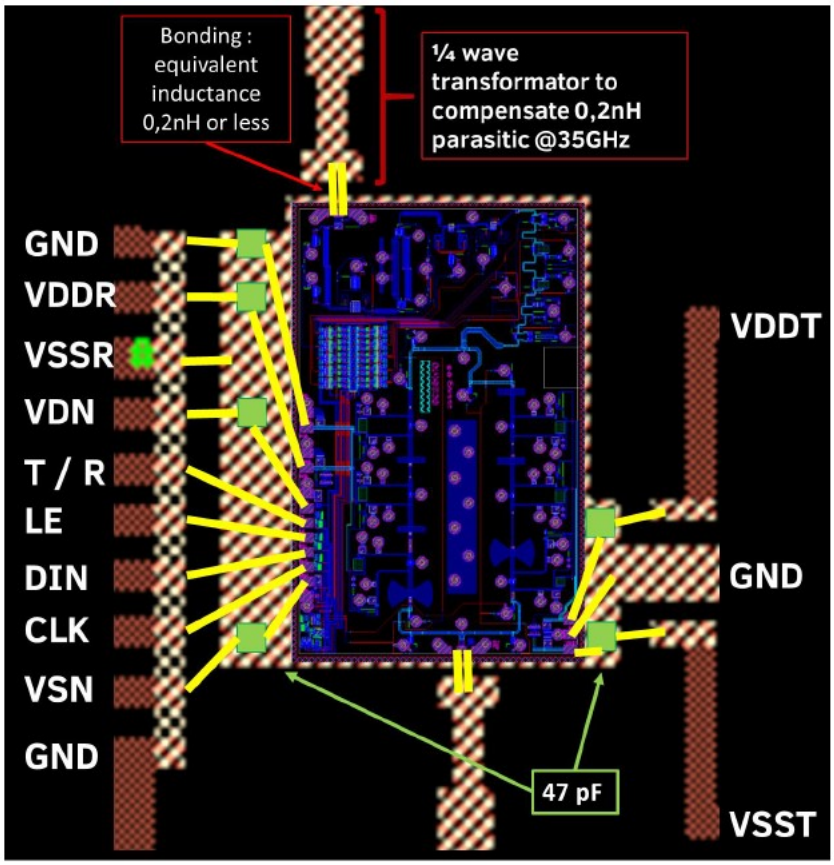
Block Diagram



Pin Configuration

Symbol	Description	Remarks
Tx In / Rx Out	RF Input for Tx, Output for Rx	—
Tx Out / Rx In	RF Output for Tx, Input for Rx	—
VDDT	transmit chain drain voltage	3.3 V to transmit 0 V to receive
VSST	transmit chain gate voltage	must be applied before VDDT / VDDR
VDDR	receive chain drain voltage	0 V to transmit 3.3 V to receive
VSSR	receive chain gate voltage	must be applied before VDDT / VDDR
VDN	control interface positive voltage	—
TR	transmit / receive control line	3.3 V to transmit 0 V to receive
LE	control interface latch enable	—
DIN	control interface data input	—
CLK	control interface clock	—
VSN	control interface negative voltage	must be applied before VDDT / VDDR
GND	all vias interconnected backside	—
Backside	ground	—

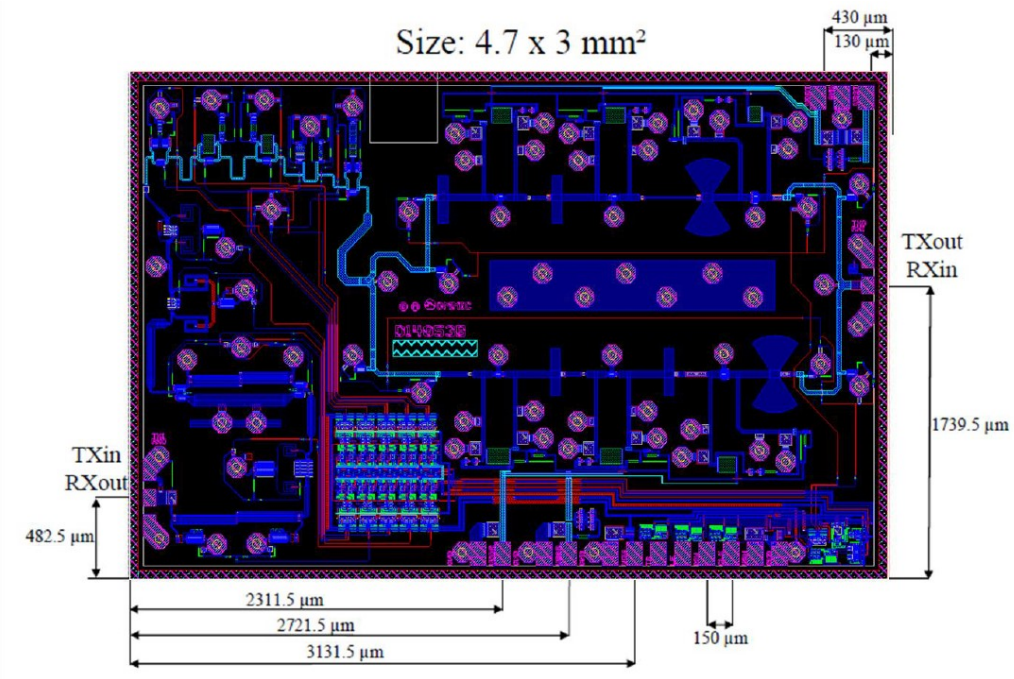
Bonding Diagram & Assembly Information



RF Bonding: 2 bonding's (wedge gold) with 25 µm in diameter and with a maximum length of 200 µm (150 µm recommended).

DC Bonding: 1 bonding with 25 µm in diameter can be used.

Mechanical Information



Chip Size = 4700 x 3000 µm (before wafer sawing)
DC Pads = 100 x 140 µm, spacing = 150 µm, top metal = Au
RF Pads = 100 x 80 µm, pitch = 150 µm, top metal = Au
Chip Thickness = 100 µm
Backside Metal = TiAu