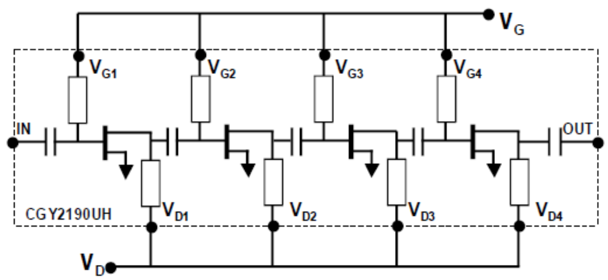
Features

- Suitable for W-Band Applications
- Wide Frequency Range: 75 - 100 GHz
- Small Signal Gain: 23 dB
- Noise Figure: 2.8 dB @ 90 GHz
- Output P1dB: 1 dBm
- Ultra Low Power consumption: (33 mW @ VD=1 & VG=0 V; 22 mW @ VD=1.2 & VG=-0.1 V)
- Chip Size: 2000 x 3000 µm
- Samples Available
- Space and MIL-STD Available
- RoHS* Compliant



Applications

- Millimeter Wave Active & Passive Imaging
- Earth Observation
- E-Band Communication
- Radar
- General Purpose

Description

The CGY2190UH/C2 is a very high performance W-band Low Noise Amplifier MMIC.

The CGY2190UH/C2 is a 4 stages Low Noise Amplifier with an exceptional Low Noise Figure of 2.8 dB at 90 GHz combined with an ultra low power consumption (VD=1 V, VG=0, total Drain current = 33 mA).

This makes the MMIC very suitable for Security Applications (Millimeter wave Imaging), Space (Earth Observation) and Telecommunications.

The MMIC is manufactured using an advanced proprietary 70 nm MHEMT technology.

Pad Configuration[1]

Pad	Function
1,3,5,8,9,11,13	GND
2	RFIN
4	No Connection
6	VD1
7	VD2
10	VD3
12	VD4
14	RFOUT

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package
CGY2190UH/C2	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Measured On Wafer, 50 Ω, Freq. = 75 - 100 GHz, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Drain Voltage	—	V	—	3.5	—
Drain Supply Current[2,3]	—	mA	—	33	—
Gate Supply Voltage	—	V	-1.0	0	+0.1
Reference Gain	75 - 90 GHz 90 - 110 GHz	dB	—	25 22	—
Input Return Loss	75 - 90 GHz 90 - 110 GHz	dB	—	-6 -6	—
Output Return Loss	75 - 90 GHz 90 - 110 GHz	dB	—	-12 -4	—
Reverse Isolation	75 - 90 GHz	dB	—	-35	—
Noise Figure[4]	90 GHz 75 - 110 GHz	dB	—	2.8 —	— 3.3
P1dB	—	dBm	—	1	—
Microwave Stability Factor	—		1	—	—

2. As bias is considered to be a drain VD voltage and a drain current ID, we have VG1 determining the drain current ID1, VG2 determining the drain current ID2, VG3 determining the drain current ID3 and VG4 determining the drain current ID4. Bias currents are set in NO RF conditions.
3. Total drain current ID total = ID1 + ID2 + ID3 + ID4 with ID1 = ID2 = ID3 = ID4.

Absolute Maximum Ratings[4,5]

Parameter	Absolute Maximum
RF CW Input Power	16 dBm
Gate Voltage	-2 to +0.6 V
Drain Voltage	0 to +2 V
Drain Current	50 mA
Gate Current	10 mA
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance	TBD

Handling Procedures

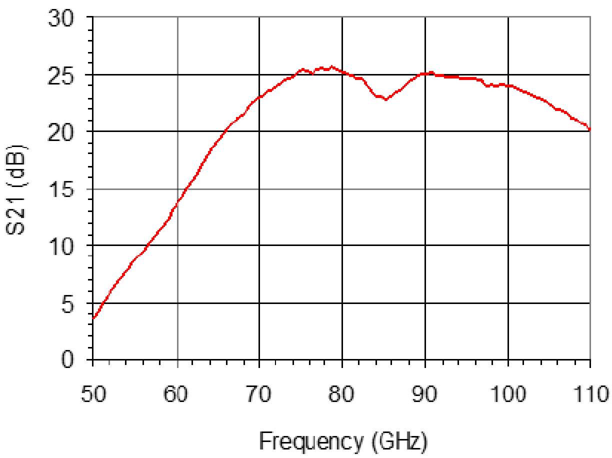
Please observe the following precautions to avoid damage:

Static Sensitivity

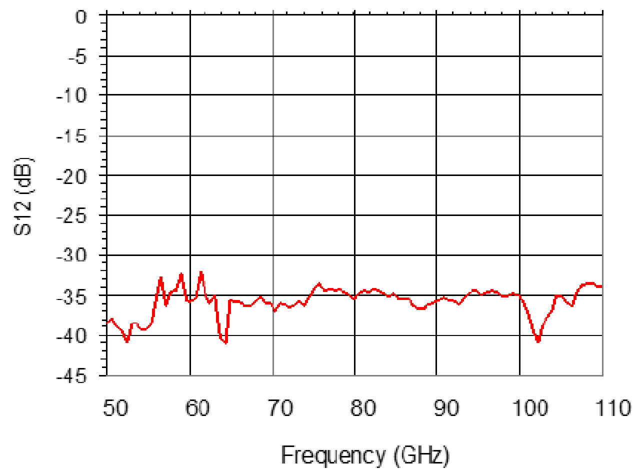
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: On Wafer Measurements

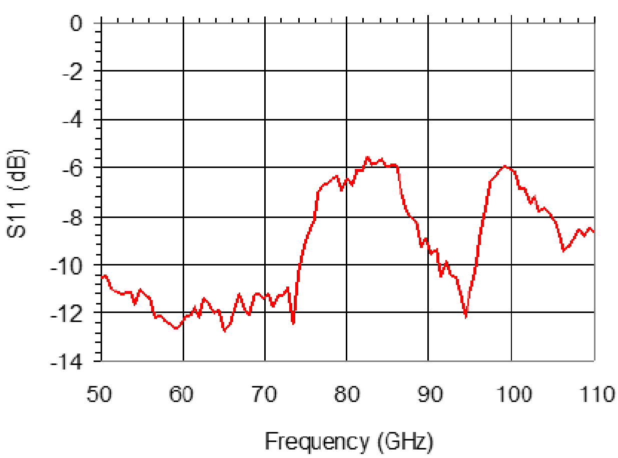
Gain vs. Frequency



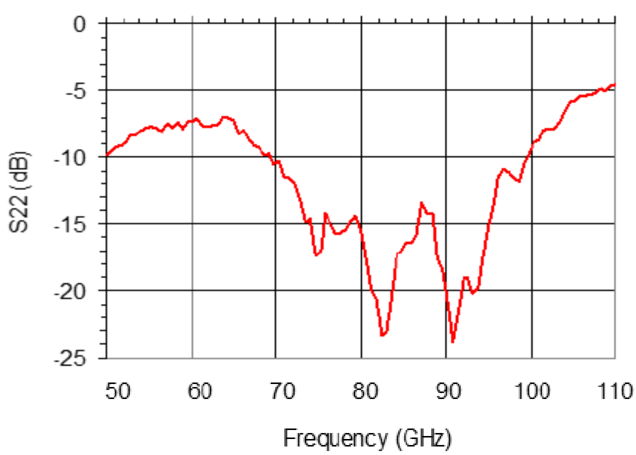
Reverse Isolation vs. Frequency



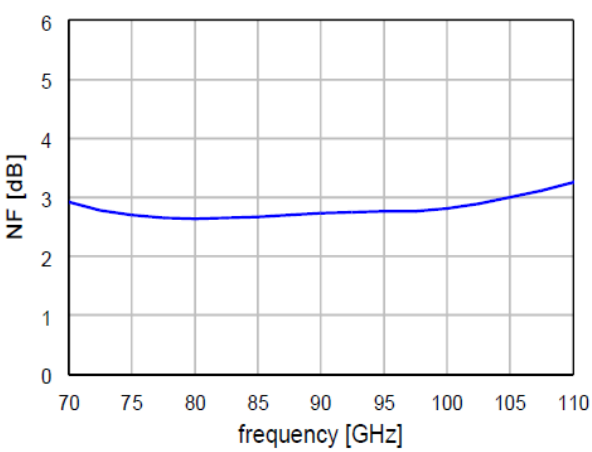
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

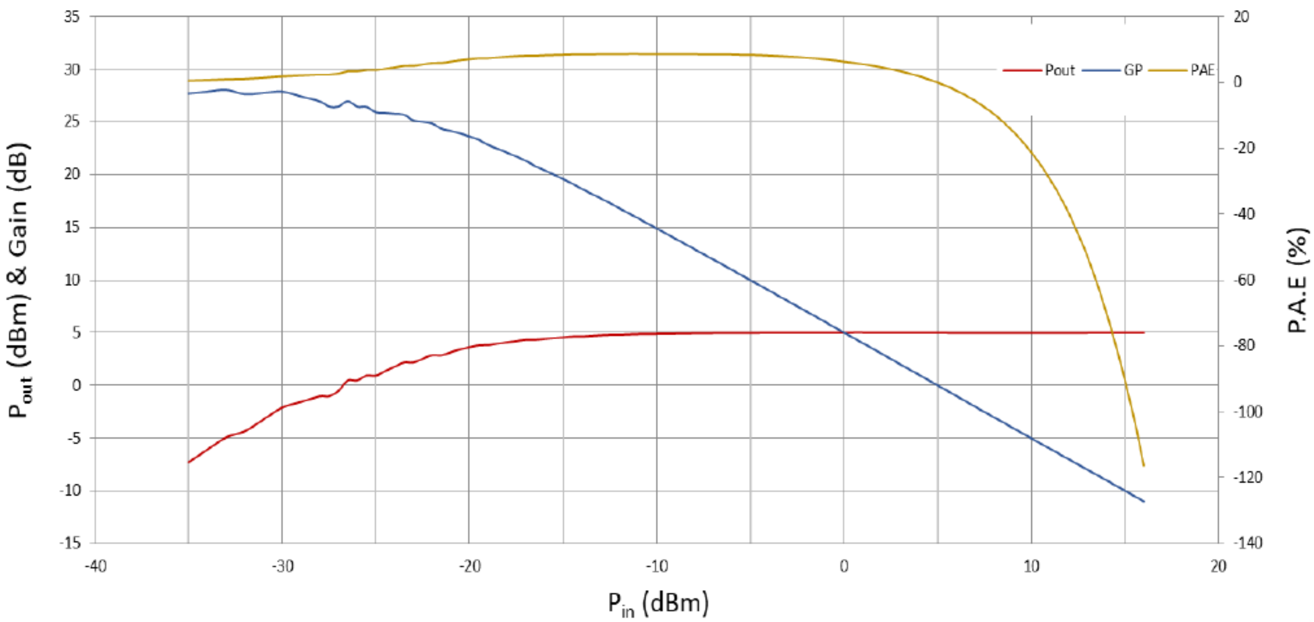


Noise Figure vs. Frequency



Typical Performance Curves: On Wafer Measurements

Output Power & Gain vs Input Power, PAE vs Input Power



Application Information (Typical application scheme)

A recommended typical module layout is proposed below. In this figure, RF input and output are using coplanar transmission lines, however, microstrip transmission lines can be used with similar performances. All path lengths and physical sizes of the components should be minimized.

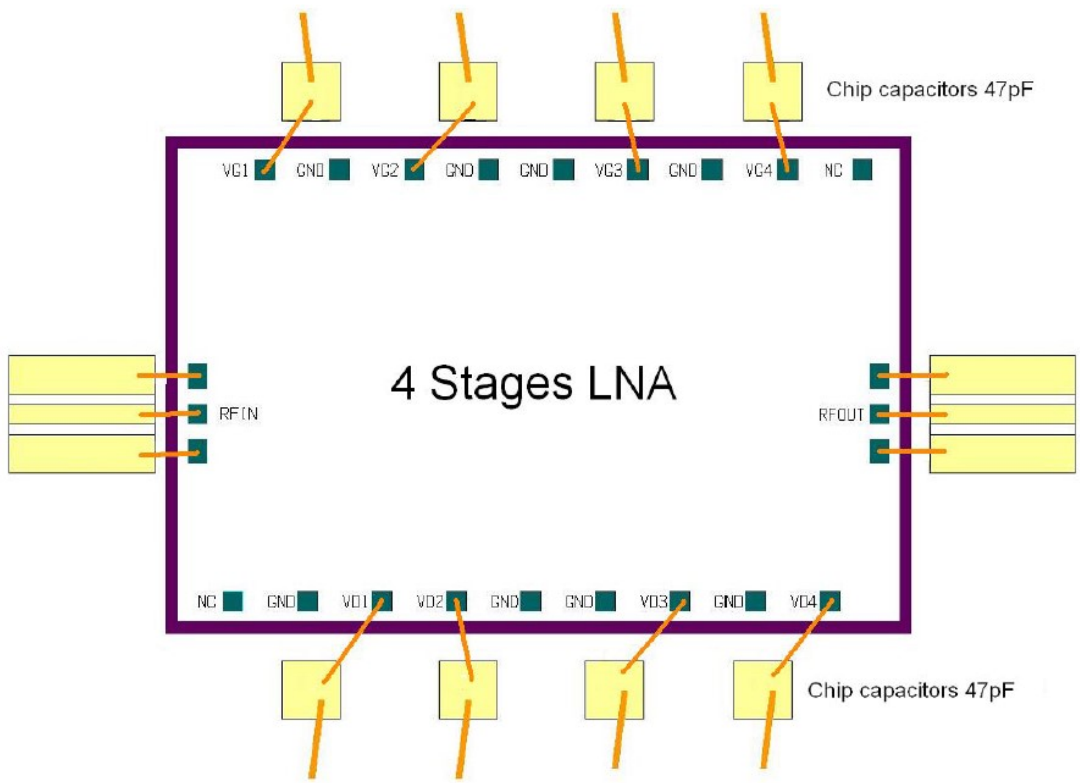
The device have been designed and optimized to support a bonding equivalent to an inductance of 80 nH to connect the 50 Ω coplanar or microstrip transmission lines. In order to minimize inductance, a Ribbon bonding technique can also be used.

All others bonding inductances (i.e. to pads VD1, VD2, VD3, VD4, and VG1, VG2, VG3, VG4) should also be kept as short as possible.

High frequency decoupling capacitors are available on-chip, external decoupling chip capacitors >47 pF and 100 nF. Surface mount capacitors are used to improve the power supply rejection. Very low frequency decoupling capacitors (1uF) can also be implemented, at very high frequencies, each transistor of the die has a very high gain.

Via holes are available on-chip to connect the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. AuSn or silver conductive epoxy material can be used for die attach.

Die Layout: Coplanar Assembly



Operating & Handling Instructions:

The CGY2190UH/C2 is a very high performance device and as such, care must be taken at all time to avoid damages due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence

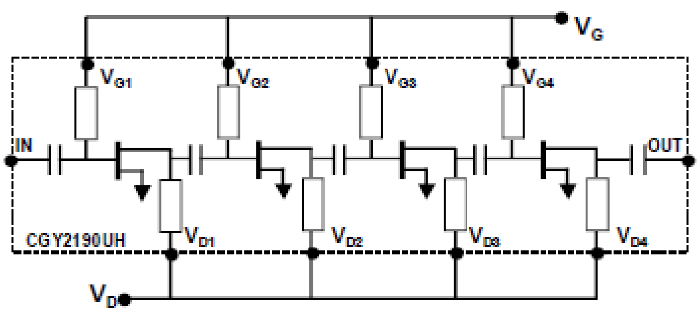
The following power supply sequence is recommended.

a) Pinch off the device by setting VG1 = VG2 = VG3 = VG4 = -1 V.
b) Increase VD = 1 V while monitoring the drain current.
c) Increase the gate voltages VG from -1 V to the value needed to reach the targeted drain current ID total = 33 mA (typically VG1 = 0 V)
d) Apply the RF input signal.

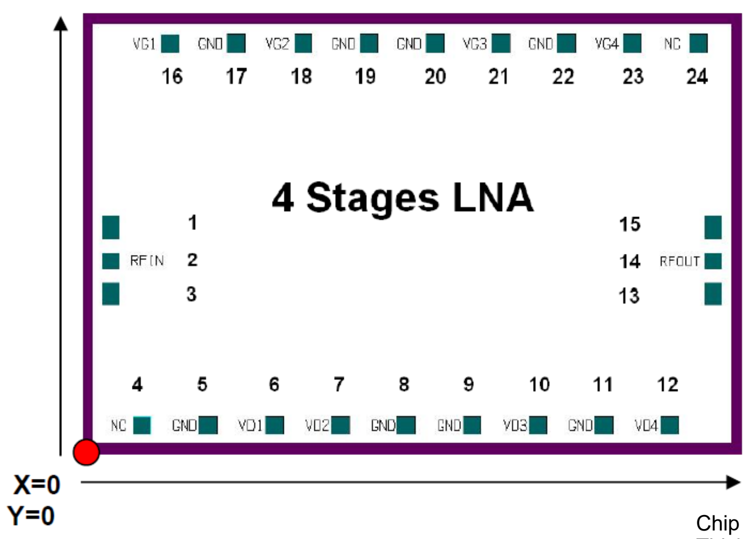
2- Mounting and ESD handling precautions

For high performance devices such as this device, care must be taken while mounting, bonding and eventually sealing the packages and hence obtain the most reliable long-term operation.

Block Diagram



Bonding Pads



Chip Size: 2000 x 3000 µm
Thickness: 100 µm
Backside Metal: TiAu
Passivation: PECVD deposited Si3N4
Bonding Pad Dimensions:
GND: 60 x 100 µm
All others:80 x 80 µm

Bonding Pad Coordinates

Pad Name	Pad Coordinate		Pad Size	Description
	X	Y		
GND	1	130	730	Connected to ground with on-chip via hole
IN	2	130	880	RF input
GND	3	130	1030	Connected to ground with on-chip via hole
NC	4	270	130	Not Connected
GND1	5	570	130	Connected to ground with on-chip via hole
VD1	6	870	130	Drain supply voltage 1
VD2	7	1170	130	Drain supply voltage 2
GND2	8	1470	130	Connected to ground with on-chip via holes
GND3	9	1770	130	Connected to ground with on-chip via holes
VD3	10	2070	130	Drain supply voltage 3
GND4	11	2370	130	Connected to ground with on-chip via holes
VD4	12	2670	130	Drain supply voltage 4
GND	13	2870	730	Connected to ground with on-chip via hole
OUT	14	2870	880	RF Output
GND	15	2870	1030	Connected to ground with on-chip via hole
VG1	16	400	1860	Gate supply voltage 1
GND	17	700	1860	Connected to ground with on-chip via hole
VG2	18	1000	1860	Gate supply voltage 2
GND	19	1300	1860	Connected to ground with on-chip via hole
GND	20	1600	1860	Connected to ground with on-chip via hole
VG3	21	1900	1860	Gate supply voltage 3
GND	22	2200	1860	Connected to ground with on-chip via hole
VG4	23	2500	1860	Gate supply voltage 4
NC	24	2800	1860	Not Connected

6. All x and y coordinates in µm represent the position of the center of the pad with respect to the lower left corner of the chip layout (see the bonding pattern).
7. Must be decoupled to ground using external capacitor (s).