4-Bit, Ku-Band Core Chip
10.70 - 12.75 GHz

CGY2179UH/C1
Rev. V1

Features

- Gain: 12 dB @ 11.7 GHz
- Noise Figure: 1.9 dB @ 11.7 GHz
- RMS Phase Error: 7° @ 11.7 GHz
- RMS Amplitude Error: 0.6 dB @ 11.7 GHz
- Output P1dB: 3 dBm
- Input Return Loss: -15 dB @ 11.7 GHz
- Output Return Loss: -12 dB @ 11.7 GHz
- Total Power Consumption: 200 mW
- Chip Size: 2.12 x 2.43 x 0.1 mm
- Tested 100%
- Samples & Demo Boards Available
- RoHS* Compliant

Applications

- Radar, Antennas
- Telecommunication
- Instrumentation

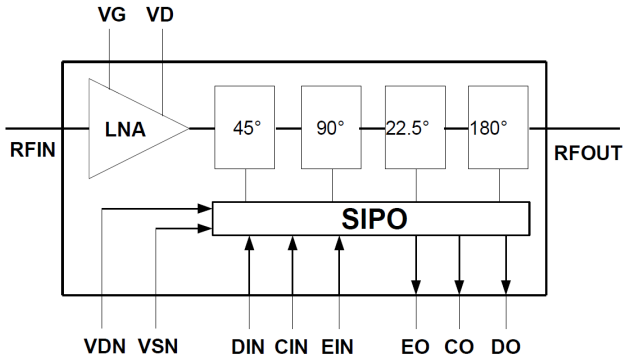
Description

The CGY2179UH/C1 is a high performance 4-bit Core Chip operating in Ku-band. It includes a 4-bit phase shifter and a LNA. It has a phase shifting range of 360°, and a LSB of 22.5°. It covers the frequency range from 10.7 to 12.75 GHz.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

This die is manufactured using 0.18 µm gate length pHEMT Technology ED02AH. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2179UH/C1	Bare Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications[1,2]: Freq. = 11.7 GHz, V_D = +2 V, V_G = -0.3 V, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	Positive Negative Drain	V	+4.5 -5.5 +1.8	+5.0 -5.0 +2.0	+5.5 -5.5 +2.2
Current	Positive Negative Drain (V_G = -0.3 V)	mA	—	12 5 55	—
Gain	—	dB	10	12	—
Noise Figure	@ Reference State	dB	—	1.9	—
Input Return Loss	All States	dB	—	-15	—
Output Return Loss	All States	dB	—	-12	—
Phase Range	—	°	—	360	—
RMS Phase Error	with regards to the 16 phase states	°	—	7	—
RMS Gain Variation	with regards to the 16 phase states	dB	—	0.6	—
P1dB	—	dB	—	3	—
Serial Data Rate	—	Mbps	—	10	—

1. The RMS value is the root mean square of the error defined as below:
2. Where x_i is the difference between the measured value and the theoretical value, x_i is the mean value of the N x_i, and σxi is the standard deviation of x_i.

$$x_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\bar{x}_i^{\,2} + \sigma_{x_i}^2}$$

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Supply Voltage Positive Negative Digital Drain Gate	 -1 V to +6 V -6 V to +1 V -1 V to +6 V -1 V to +3 V -0.4 V to 0 V
Input Power	0 dBm
Junction Temperature	+150°C
Storage Temperature	-55°C to +150°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Operating Conditions

Parameter	Absolute Maximum
Supply Voltage Positive Negative Digital Drain Gate	 0 V to +5 V -5 V to 0 V 0 V to +5 V 0 V to +2 V -0.4 V to 0 V
Input Power	0 dBm
Operating Temperature	-40°C to +85°C

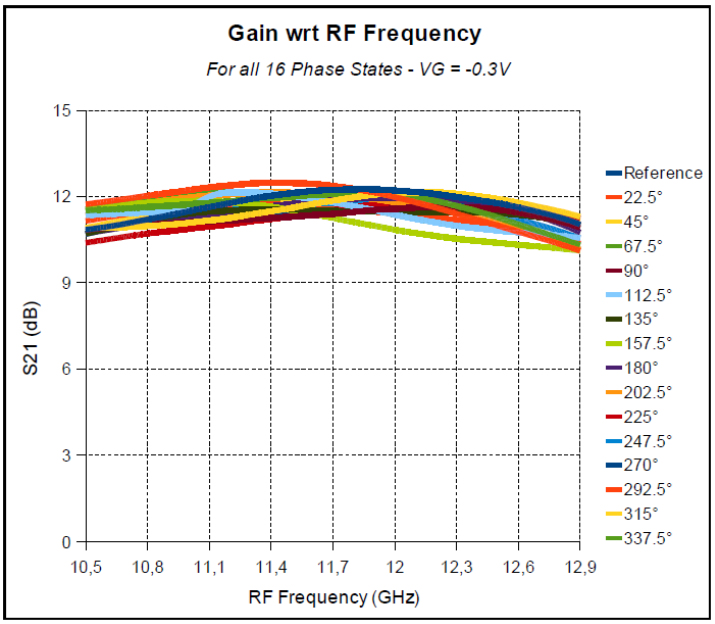
Handling Procedures

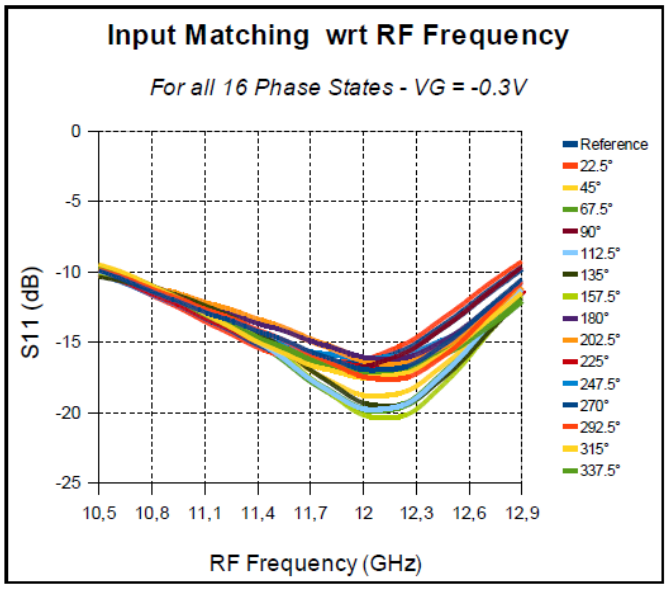
Please observe the following precautions to avoid damage:

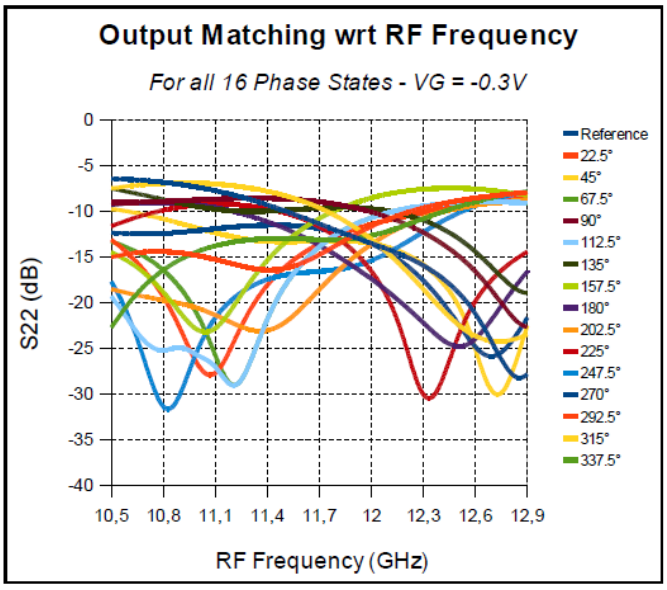
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: On Wafer Measurements







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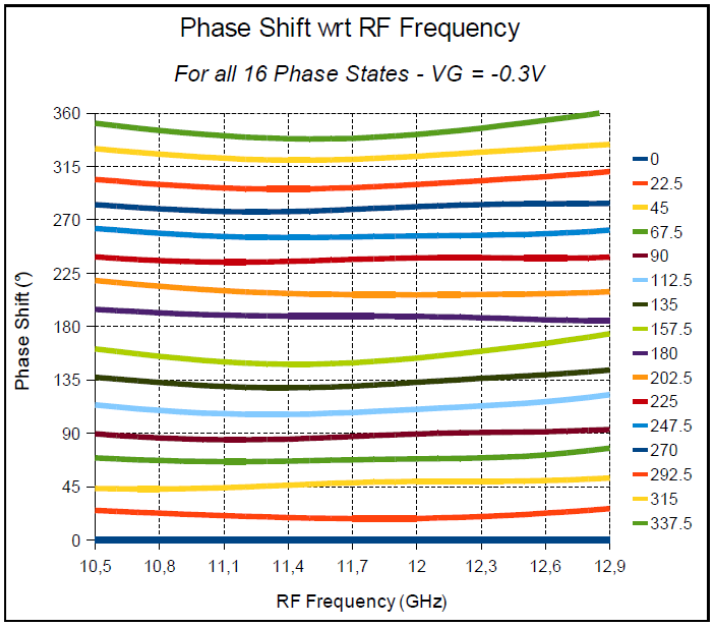

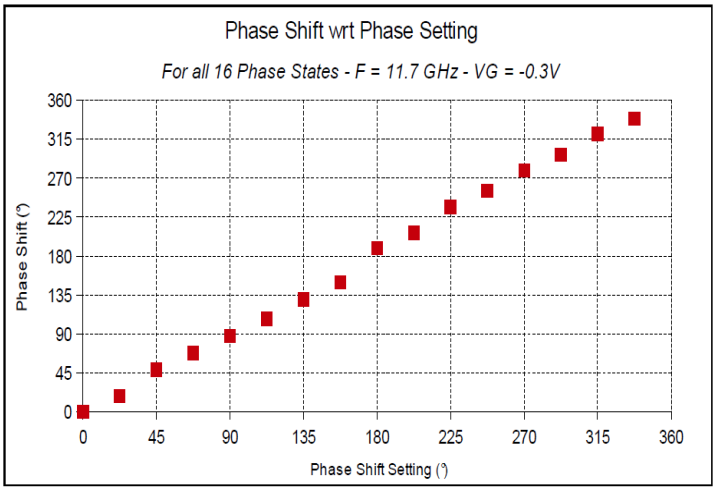

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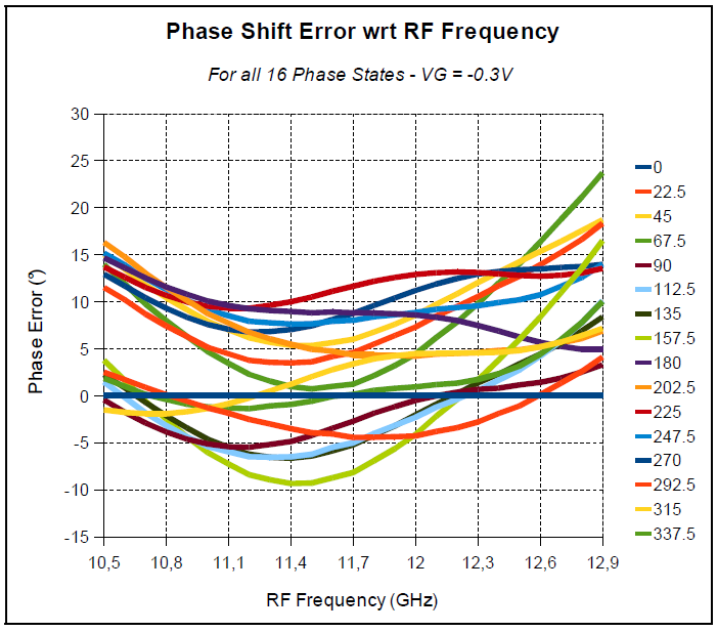

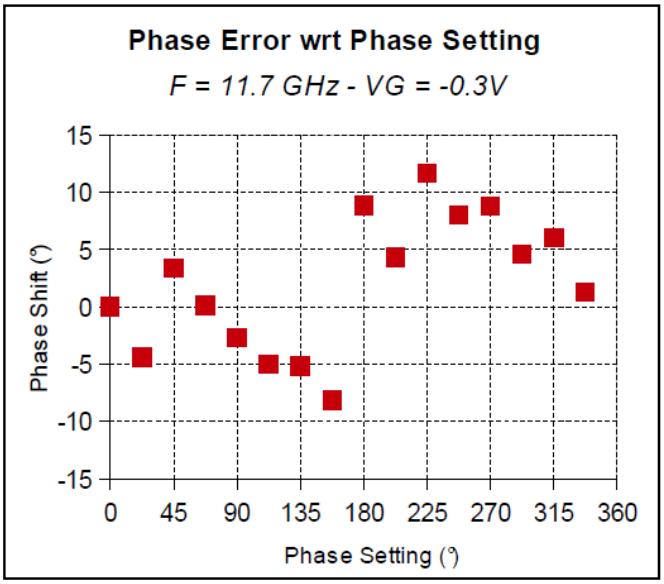

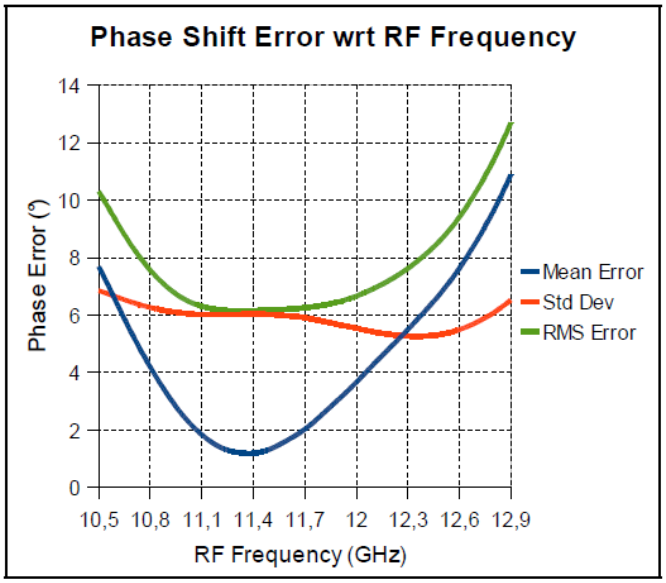

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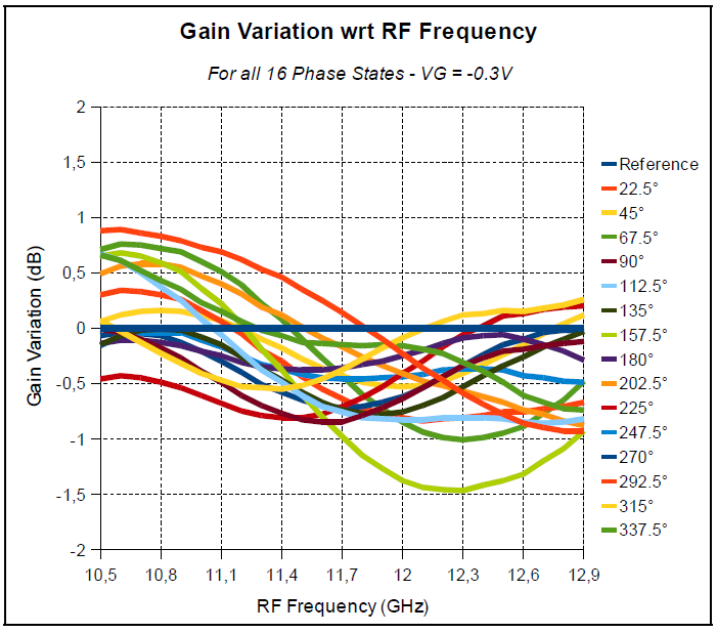
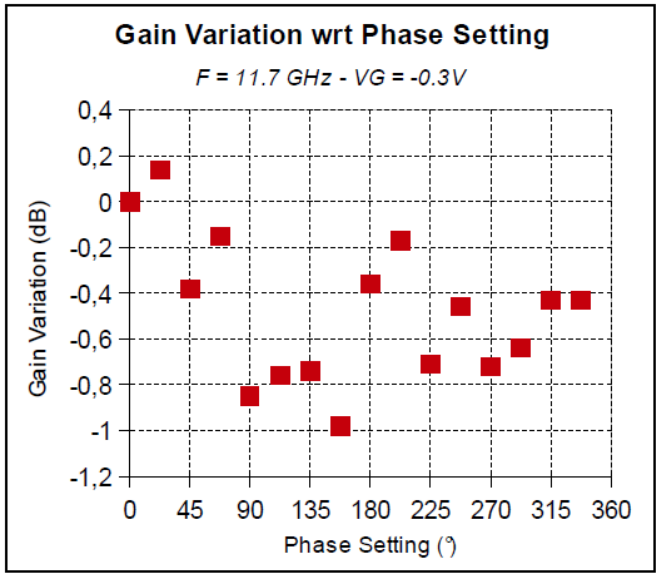
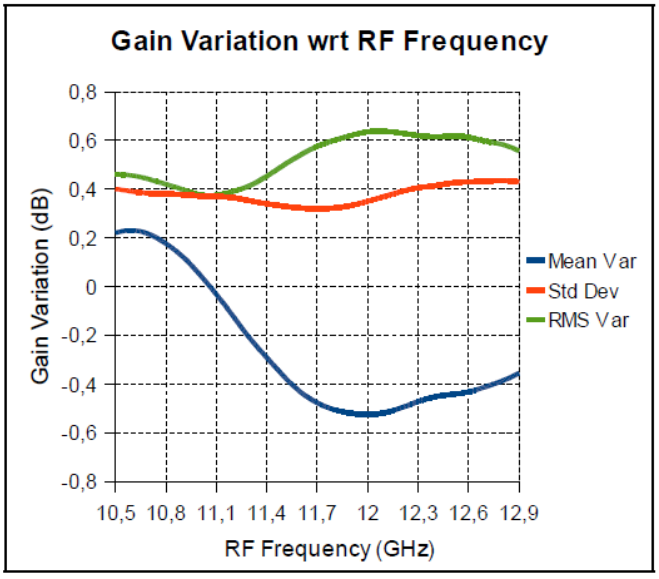






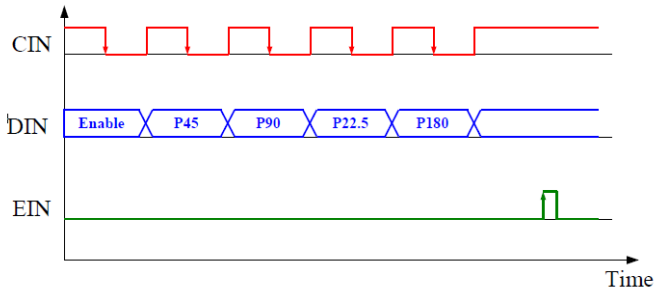
Data (Reference State LOW)

Bit #	Description	Theoretical Value
B0	Enable	—
B1	45° Phase Shifting Cell	45°
B2	90° Phase Shifting Cell	90°
B3	22.5° Phase Shifting Cell	22.5°
B4	180° Phase Shifting Cell	180°

Control Voltage (CMOS Standard Logic)

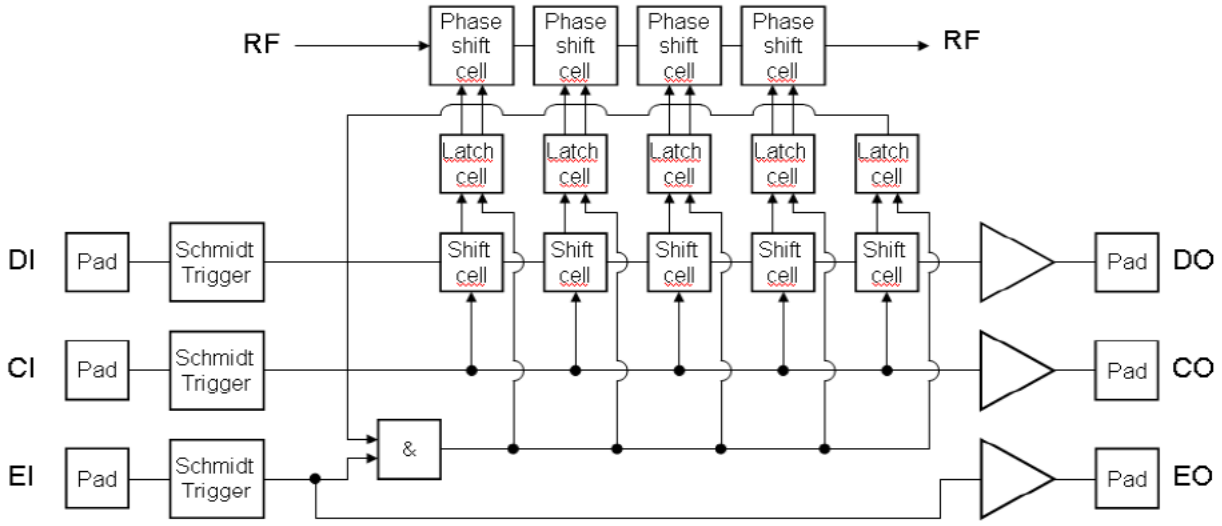
State	V Min.	V max.
Low	0 V	1 V
High	3 V	V_{DN}

Timing Diagram



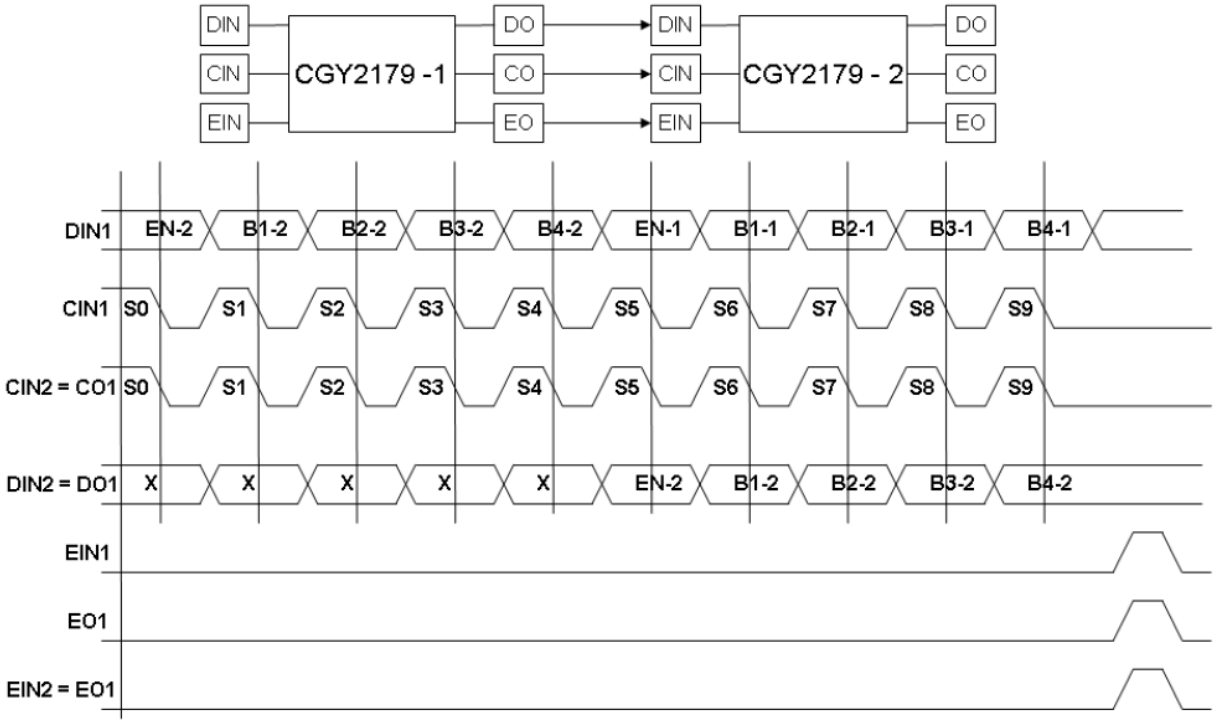
- DIN is sampled at the falling edge of CIN.
- Falling edge of EIN must occur when all the 5 bits are loaded and on high level of CIN.
- DIN is transferred and Phase Shifter positions changed on high level of EIN.

Internal Control Block Diagram



Cascaded CGY2179UH/C1 Control
2 or more CGY2179UH/C1 can be cascaded and controlled by a unique serial interface.

The enable/disable bit and associated internal hardware allow the user to chose the devices which are not subject to reprogramming in the device chain.

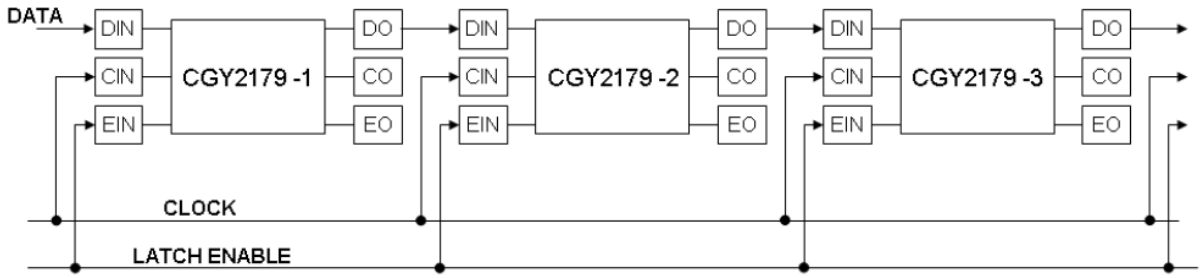


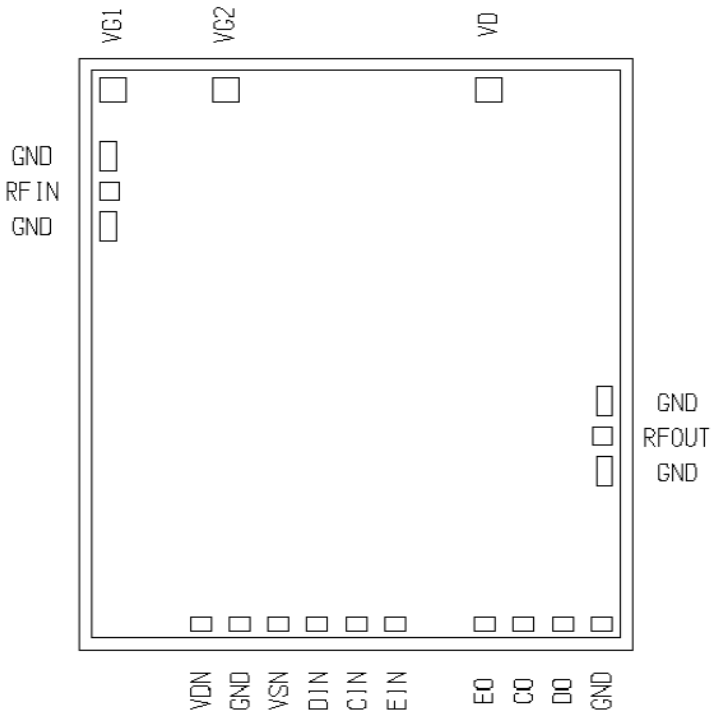
Daisy Chain Configuration

An alternate way of designing a multiple CGY2179UH/C1 system using a single serial interface is to use the daisy chain mechanism.

Output data pin DO of device number N is connected to Input data pin DIN of device number N+1, Clock and LATCH ENABLE pin are driven in parallel.

The enable/disable bit and associated internal hardware allow the user to chose the devices which are not subject to reprogramming in the device chain.



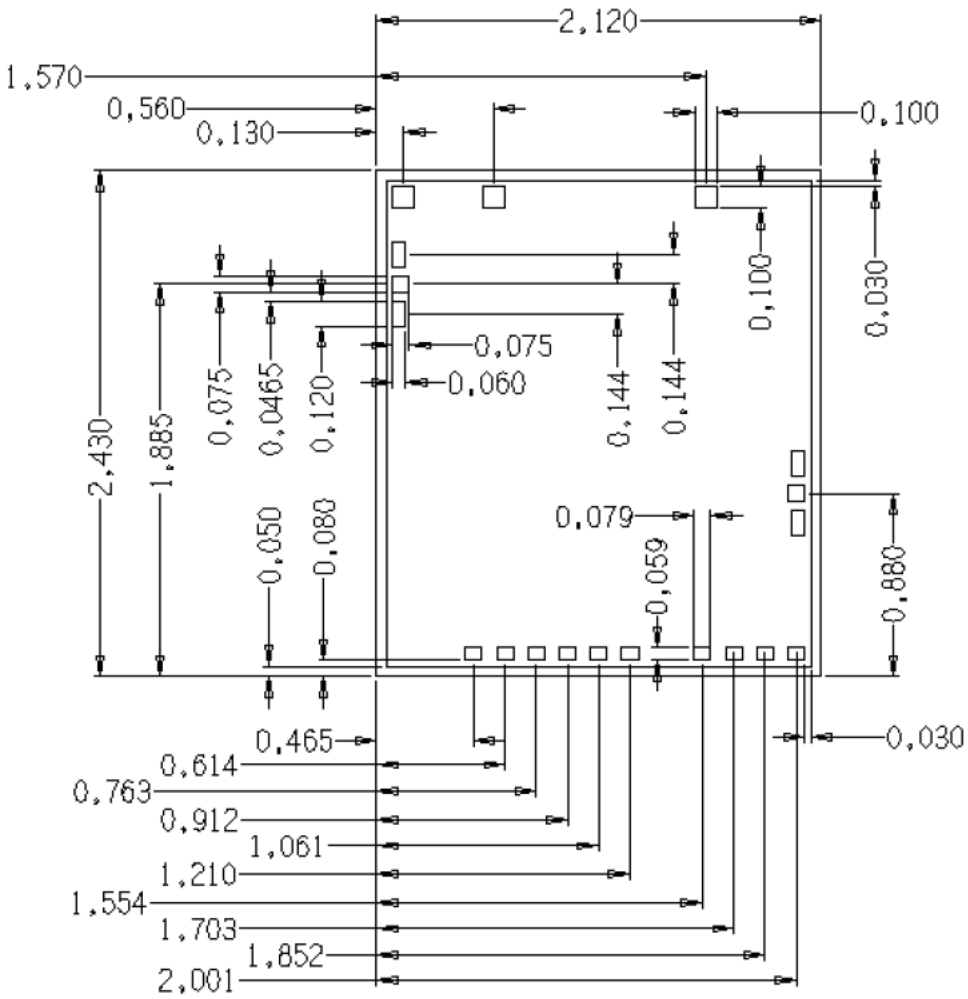


Pin Configuration[5]

Pin #	Symbol	Description
1,5,6,20 - 23,25,26,28	GND	Ground
2,4,8,16,17,19	RFIN	RF Input
3	VDN	Positive Supply Voltage
7	VSN	Negative Supply Voltage
9	DIN	Data Input
10	CIN	Clock Input
11	EIN	Enable Input
12	EO	Data Output
13	CO	Clock Output
14	DO	Enable Output
15	RFOUT	RF Output
18	VD	Drain Voltage
24	VG1	Gate Voltage 1st Stage LNA
27	VG2	Gate Voltage 2nd Stage LNA

5. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Mechanical Information



Notes 1 : RFIN and RFOUT pads are suitable to accommodate GSG 150 mm RF probes
- – Central pad (Signal) is 75 x 75 mm
- – Lateral pads (GND) are 120 x 60 mm
- – Distance from central pad to ground pads are 46.5 mm
- – Distance from pad to dicing streets are 30 mm

Notes 2 : Control pad
- – North pads are 100 x 100 mm
- – South pads are 79 x 49 mm
- – Distance from pad to dicing streets are 30 mm

Notes 3 : Dicing reduce the device by approximately 32 mm