

Low Noise Amplifier, C-Band, High Gain 5 - 6 GHz



CGY2178UH/C1

Rev. V1

Features

- C-band MMIC LNA
- S11, S22:
 - <-15 dB (7.5% Bandwidth)
 - < -10 dB (5 - 6 GHz)
- Noise Figure: 1 dB
- Gain: 30 dB
- OIP3: 22 dBm
- Output P1dB: 15 dBm
- Circuit Size: 1.5 mm x 1.6 mm, 100 μ m thick
- 100% RF Tested, Known Good Die
- Uses a highly reliable pHEMT MMIC process
- Demonstration Boards Available
- Samples Available
- RoHS* Compliant

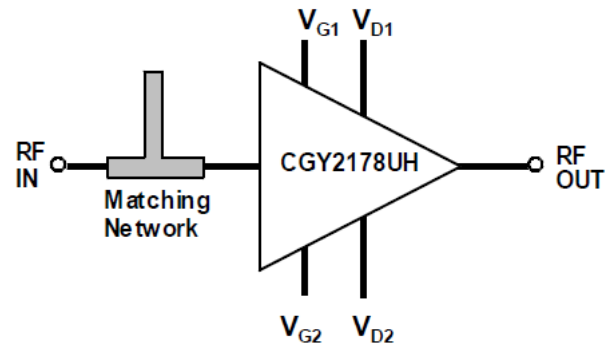
Applications

- C-Band Active Antennas
- General Purpose

Description

The CGY2178UH/C1 is a high gain, low noise figure MMIC amplifier designed for use with the integrated core chip, attenuator/phase shifter chip set or as a general purpose low noise amplifier in band C. The CGY2178UH/C1 uses a simple external matching circuit to provide excellent input matching and low noise figure between 5 and 6 GHz. All biasing, decoupling and output-matching networks are on chip.

The MMIC is manufactured with a 0.18 μ m PHEMT GaAs MMIC technology. The device is fully passivated.



Ordering Information

Part Number	Package
CGY2178UH/C1	MMIC C-Band LNA

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**Electrical Specifications¹: Measured On Reference Board,
Freq. = 5.3 GHz, $V_{D1} = V = 3$ V, $I_{D1} = 10$ mA, $I_{D2} = 30$ mA, $T_A = +25^\circ\text{C}$**

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	—	30	—
Noise Figure	—	dB	—	1.05	—
Reverse Isolation	Out/In	dB	—	40	—
Output IP3	—	dBm	—	22	—
Output P1dB	—	dBm	—	15	—
Input Return Loss	50 Ω Source	dB	—	-15	—
Output Return Loss	50 Ω Load	dB	—	-15	—

1. Measurement reference planes are the INPUT and OUTPUT SMA connectors.

Absolute Maximum Ratings^{2,3}

Parameter	Absolute Maximum
Input Power	5 dBm
Gate Voltage ⁴ Stage 1 & Stage 2	-6 to 0 V
Drain Voltage Stage 1 & Stage 2	0 to +6 V
Drain Current Stage 1	40 mA
Stage 2	60 mA
Gate Current	10 mA
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- VD1 Open Circuited

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance	235°C/W

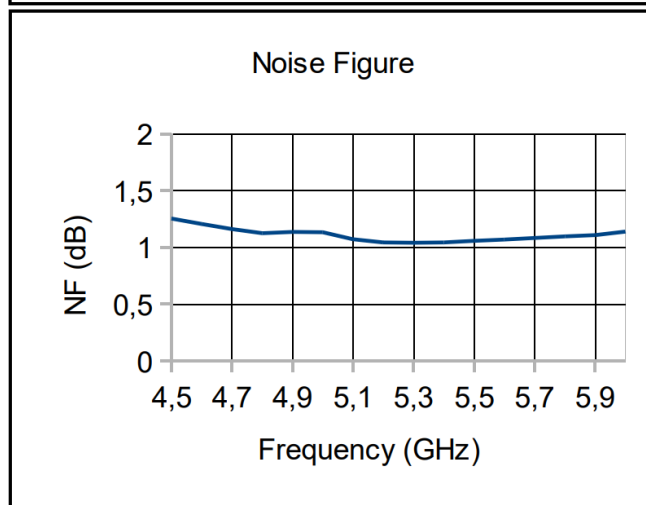
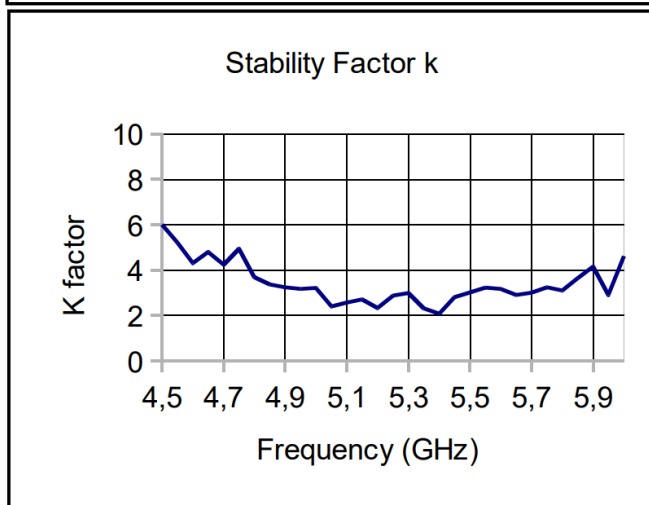
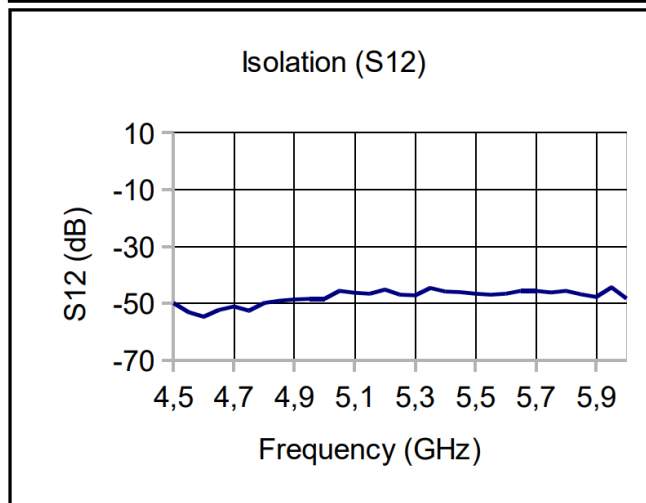
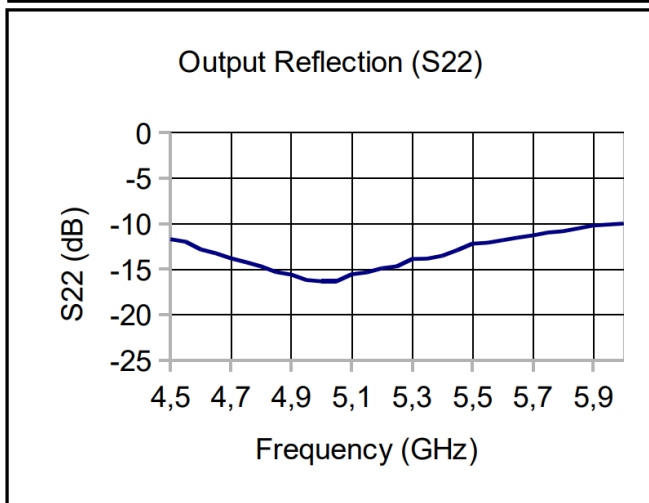
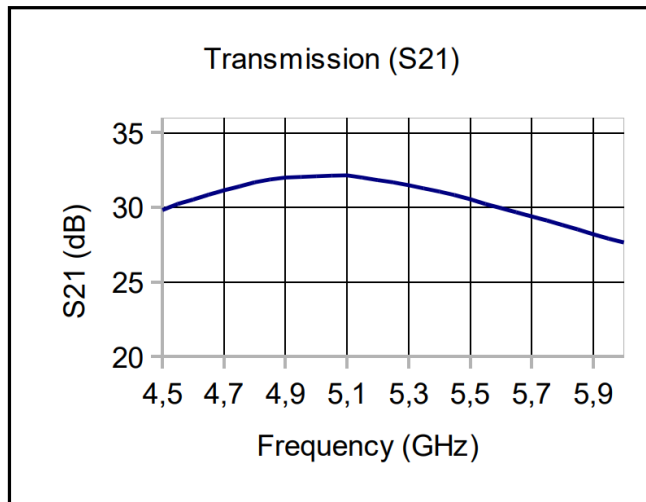
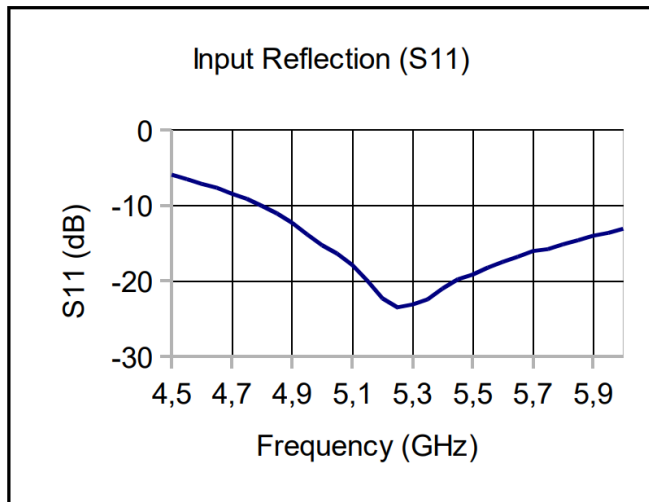
Handling Procedures

Please observe the following precautions to avoid damage:

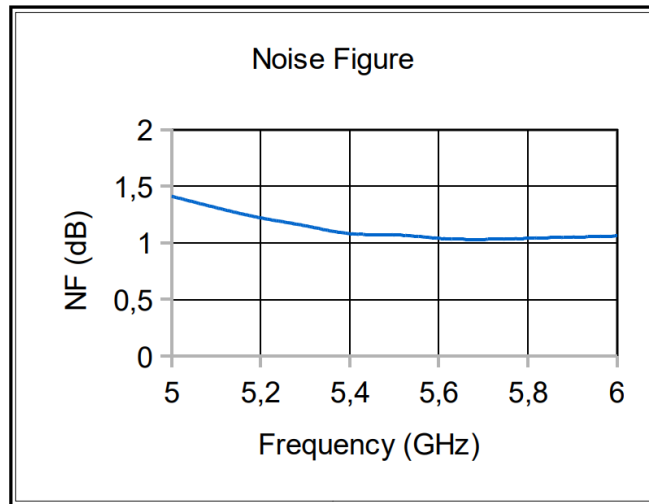
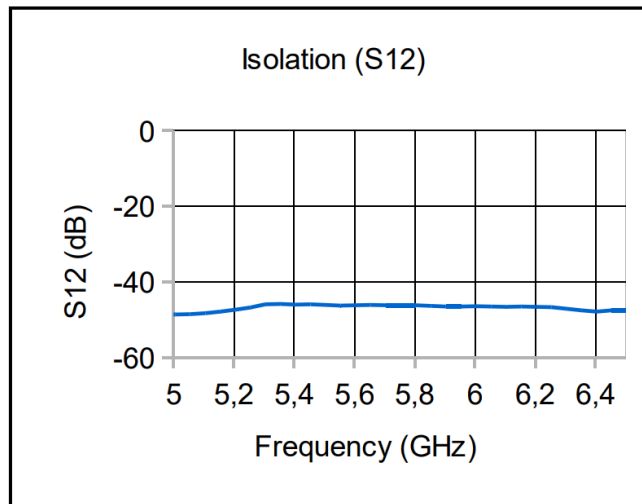
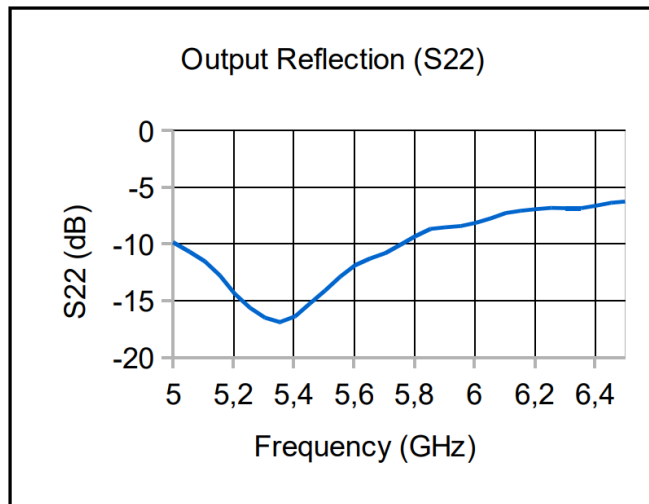
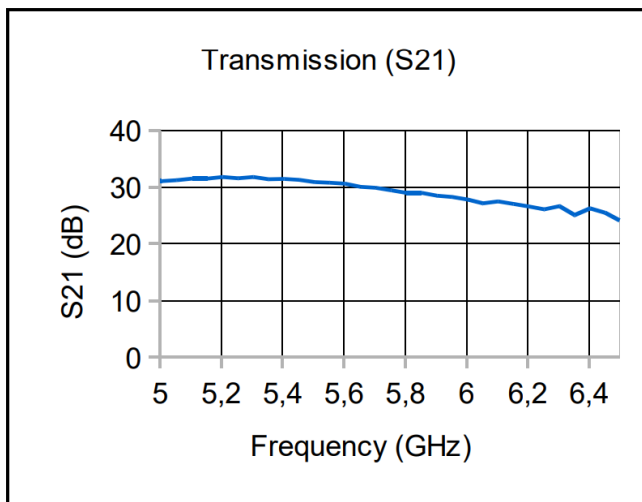
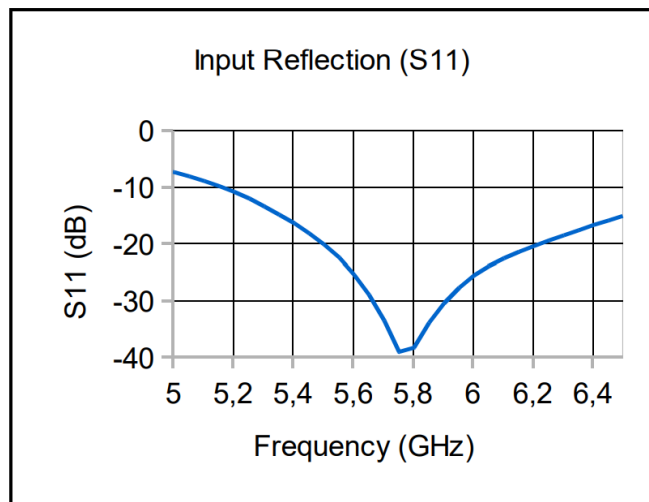
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: 5.3 GHz Optimized

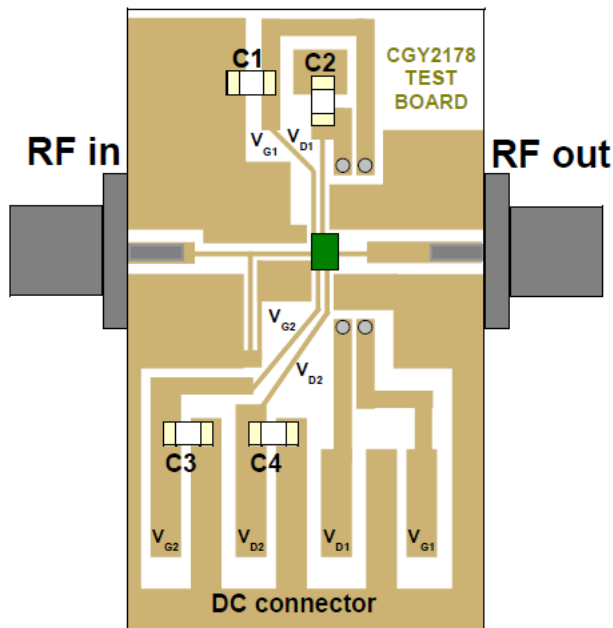


Typical Performance Curves: 5.8 GHz Optimized



Reference Board

Assembly drawing



Bill of materials

INPUT matching (see note 1):

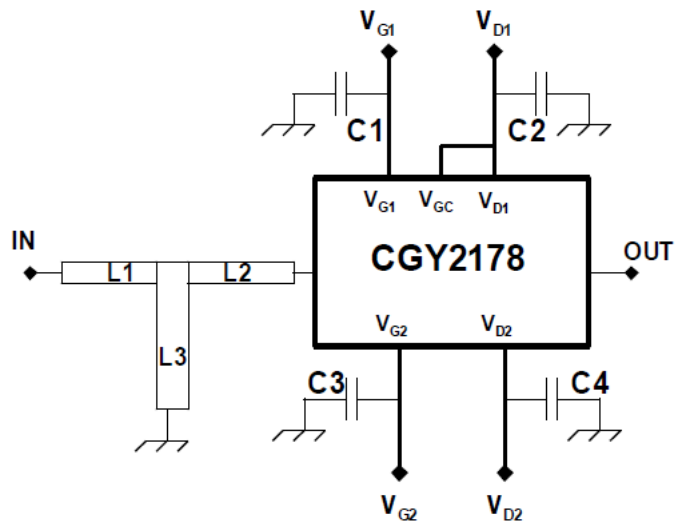
Optimised for 5300 MHz. L1, L2 and L3 are coplanar transmission lines.

Component	Length (μm)	Width (μm)	Gap (μm)
L1	2600	200	200
L2	3500	200	200
L3	4000	200	200

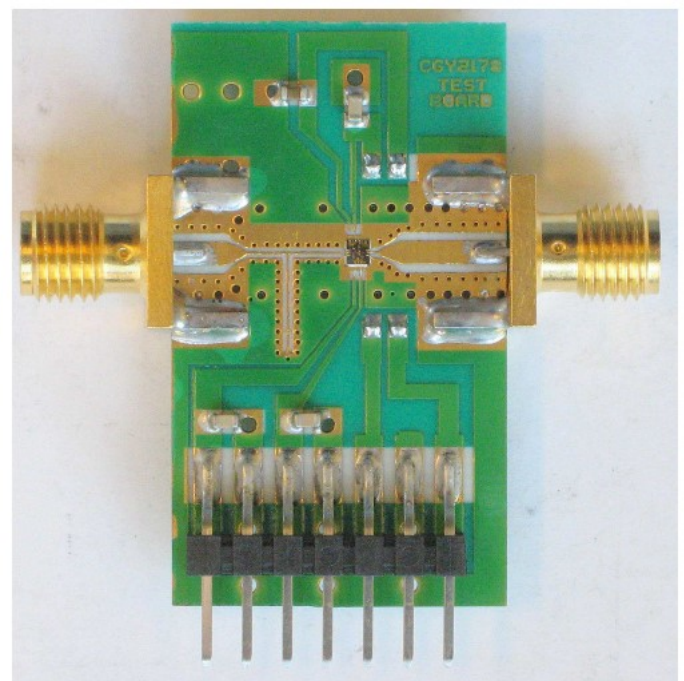
Note 1: Dimensions are given for Rogers RO4003 substrate material. (Height = 800 μm , $E_r = 3.4$).

Component	Value	Reference
C1, C2, C3, C4	100 nF	0603

Circuit Diagram



CGY2178UH Reference Board



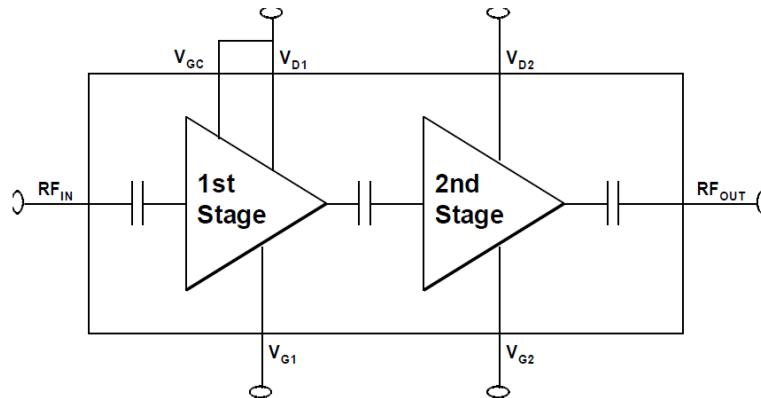
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Block Diagram



Pin Configuration

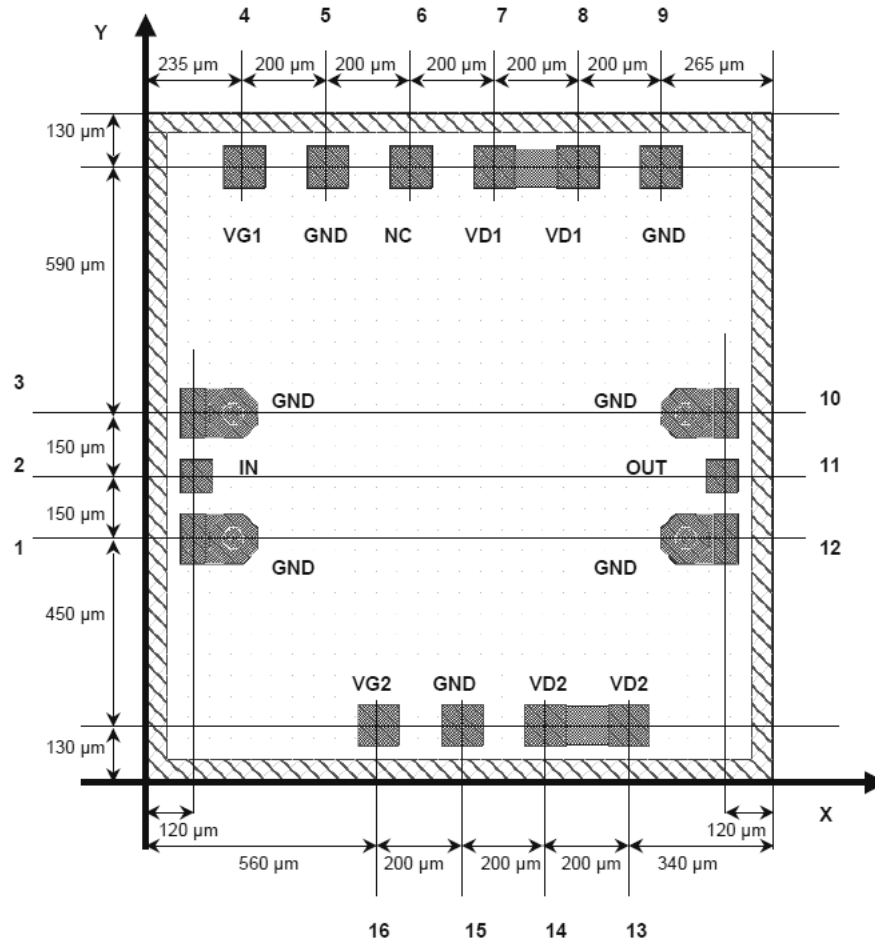
Pin #	Pin Name	Description
1,3,5,9,10,12,15	GND	Ground
2	IN	RF Input
4	V _{G1}	Stage 1: Gate Biasing
6	V _{GC}	Connected to V _{D1}
7,8	V _{D1}	Stage 1: Drain Biasing
11	OUT	RF Output
13,14	V _{D2}	Stage 2: Drain Biasing
16	V _{G2}	Stage 2: Gate Biasing

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Mechanical Information



Chip Size: 1500 x 1600 µm (± 15 µm)
 GND, VG1, VG2, VD1, VG2, VD2: 100 x 100 µm
 In, OUT: 80 x 80 µm
 Substrate Thickness: 100 µm
 Backside Metal: TiAu
 Passivation: PECVD deposited Si₃N₄

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