# 3-Port, 6-Bits, C-Band Integrated Core Chip 4.5 - 6.5 GHz

**CGY2175AUH/C1**
**Rev. V1**

## Features

- Insertion Loss: 12 dB @ 5.4 GHz
- Phase Shift Range: 360°
- Attenuation Range: 31.5 dB
- RMS Phase Error: 1.3° @ 5.4 GHz
- RMS Amplitude Error: 0.2 dB @ 5.4 GHz
- Return Loss: <-14 dB @ 5.4 GHz (All States)
- Total Power Consumption: 0.1 W
- Chip Size: 3765 x 4465 µm ±5 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space & MIL-STD Available
- RoHS* Compliant

## Applications

- Radar
- Telecommunication
- Instrumentation

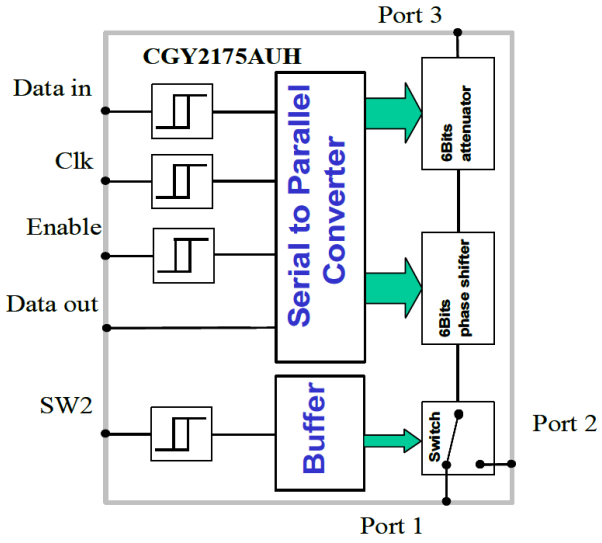
## Description

The CGY2175AUH/C1 is a high performance GaAs pHEMT technology MMIC 3 port, 6–bit Core Chip operating in C-band. It includes a 6-bit phase shifter, a 6-bit attenuator and T/R switch. The on-chip series to parallel converter minimizes the number of bonding pads and greatly simplifies the use of the Core Chip functions.

The die is manufactured using 0.18 µm gate length pHEMT Technology. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

## Block Diagram




## Ordering Information

| Part Number | Package |
|---|---|
| CGY2175AUH/C1 | Die |

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

## Electrical Specifications: Freq. = 5.4 GHz, $T_A$ = +25°C

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Supply Voltage | Positive<br>Negative<br>Digital Negative | V | +4.5<br>-3.25<br>-3.25 | +5.0<br>-3.00<br>-3.00 | +5.5<br>-2.75<br>-2.75 |
| Supply Current | Positive<br>Negative<br>Digital Negative | mA | — | 9<br>10<br>9 | — |
| Insertion Loss | No Attenuation | dB | — | 11.7 | — |
| Input Return Loss | Port 1 & Port 2 | dB | — | -14 | — |
| Output Return Loss | Port 3 | dB | — | -14 | — |
| Attenuation | Port 3 to Port 1<br>Port 3 to Port 2 | dB | — | 11.7<br>11.7 | — |
| Switch Isolation | Port 2 to Port 1 | dB | -40 | — | — |
| Attenuation Range | — | dB | — | 31.5 | — |
| RMS Attenuation Error[1,2] | — | dB | — | 0.18 | — |
| Attenuation Variation | — | dB | -0.2 | — | +0.7 |
| Phase Range | — | ° | — | 360 | — |
| RMS Phase Error[1,2] | — | ° | — | 1.25 | 4 |
| Phase Variation | — | ° | -3 | — | +3 |
| P1dB | No Attenuation | dBm | — | 20 | — |
| Switching Time | Rx/Tx | ns | — | 10 | — |
| Serial Data Rate | — | MHz | — | 100 | — |

1. The RMS value is the root mean square of the error defined as below:
2. Where $x_i$ is the difference between the measured value and the expected value.

$$x_{\text{rms}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \cdots + x_N^2}{N}}$$

## Absolute Maximum Ratings[3,4]

| Parameter | Absolute Maximum |
|---|---|
| Supply Voltage<br>Positive<br>Negative<br>Digital Negative | <br>-5 to +7 V<br>-5 to +5 V<br>-5 to +5 V |
| Digital Data Input | -5 to +7 V |
| Input Power<br>@ RF Port 1 & Port 2 | 25 dBm |
| Junction Temperature | +150°C |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +150°C |

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

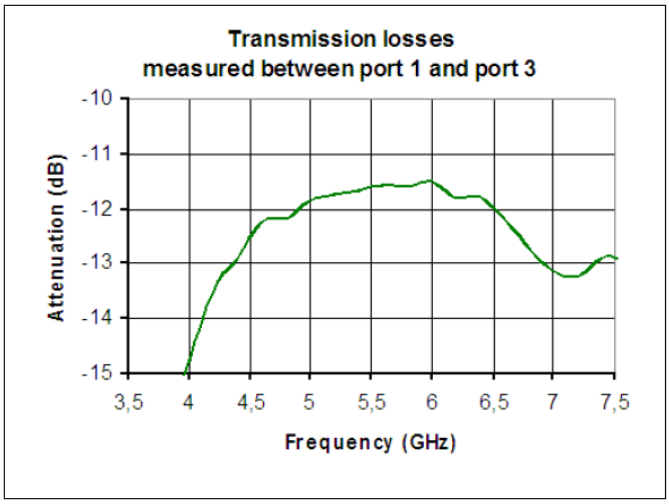
## Handling Procedures

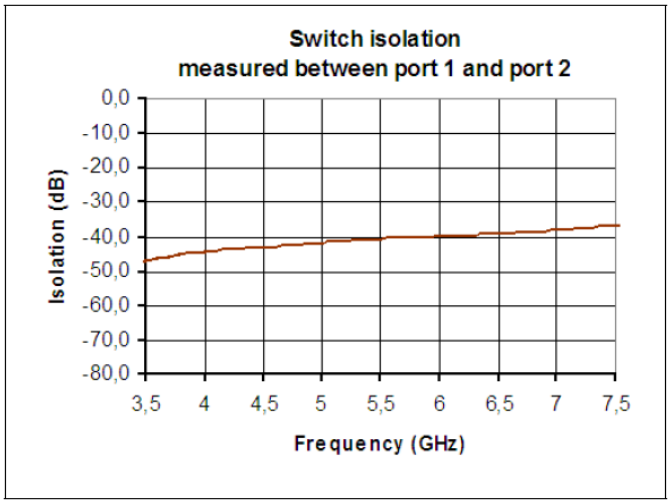
Please observe the following precautions to avoid damage:

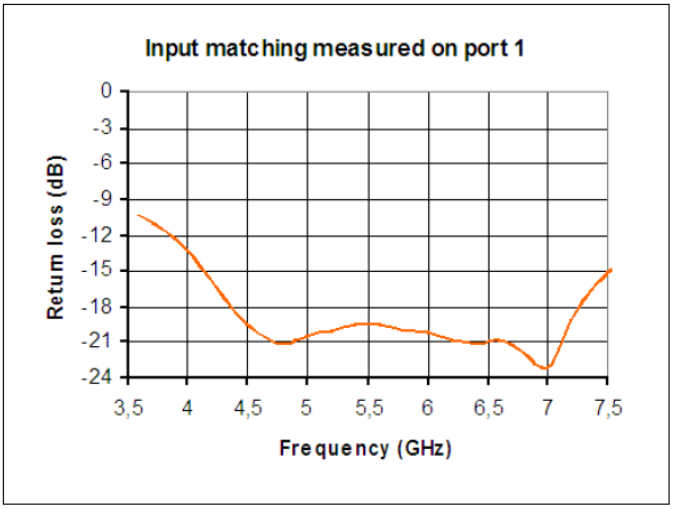
## Static Sensitivity

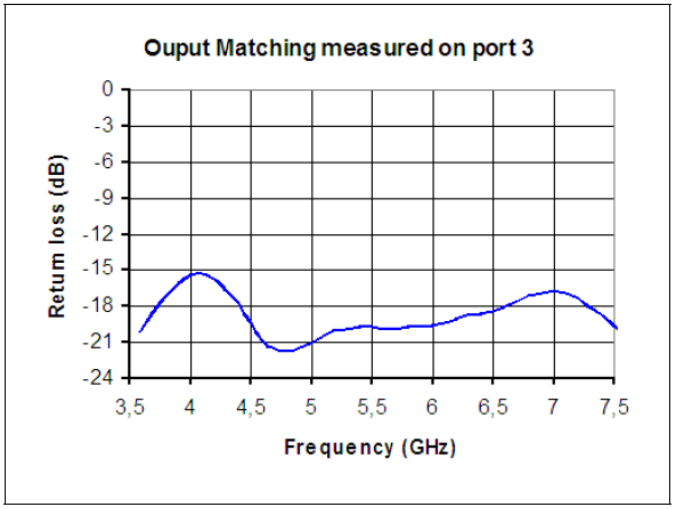
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

## Typical Performance Curves: Measured on Reference State @ $T_A$ = 25°C ; $V_{DD}$ = 5 V ; $V_{CC1}$ = $V_{CC2}$ = -3 V; SW2 = +5 V



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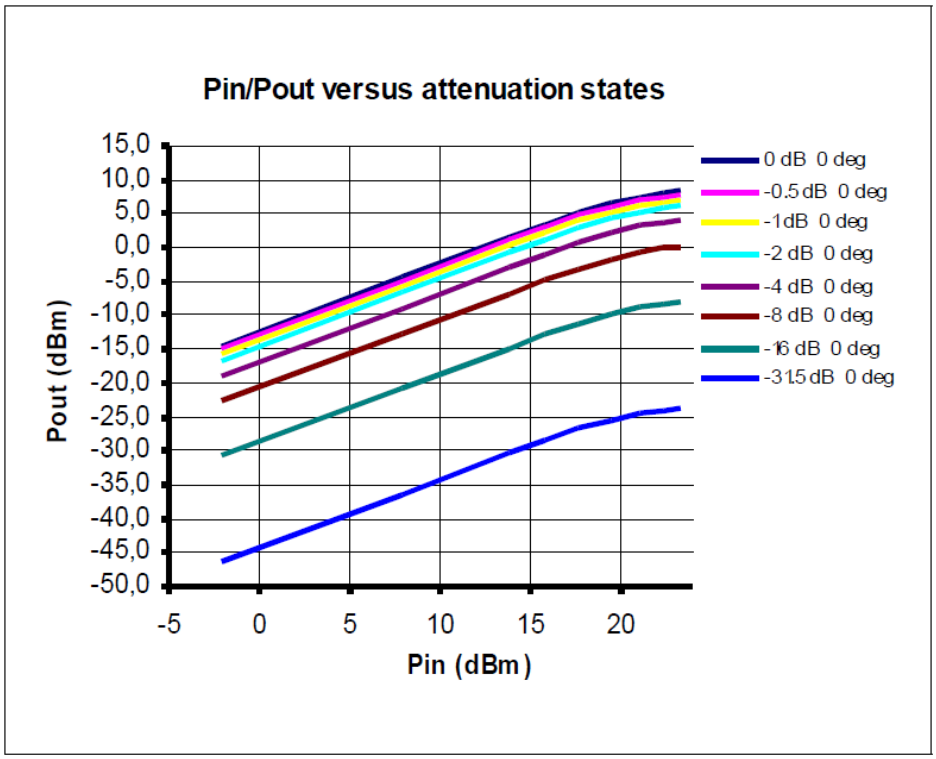


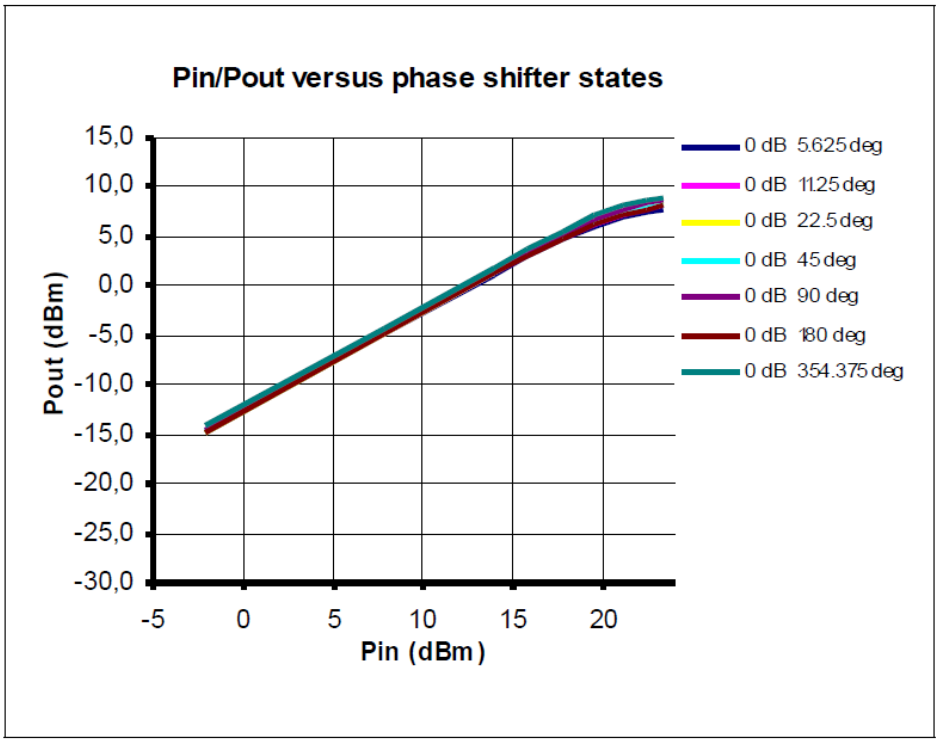

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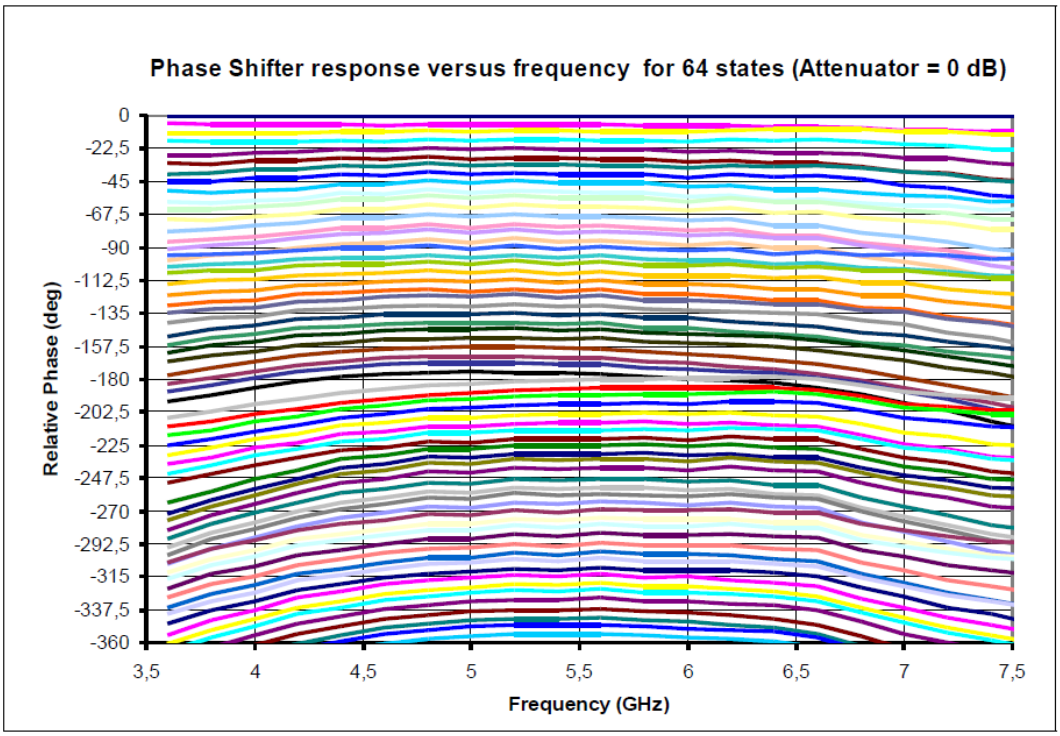


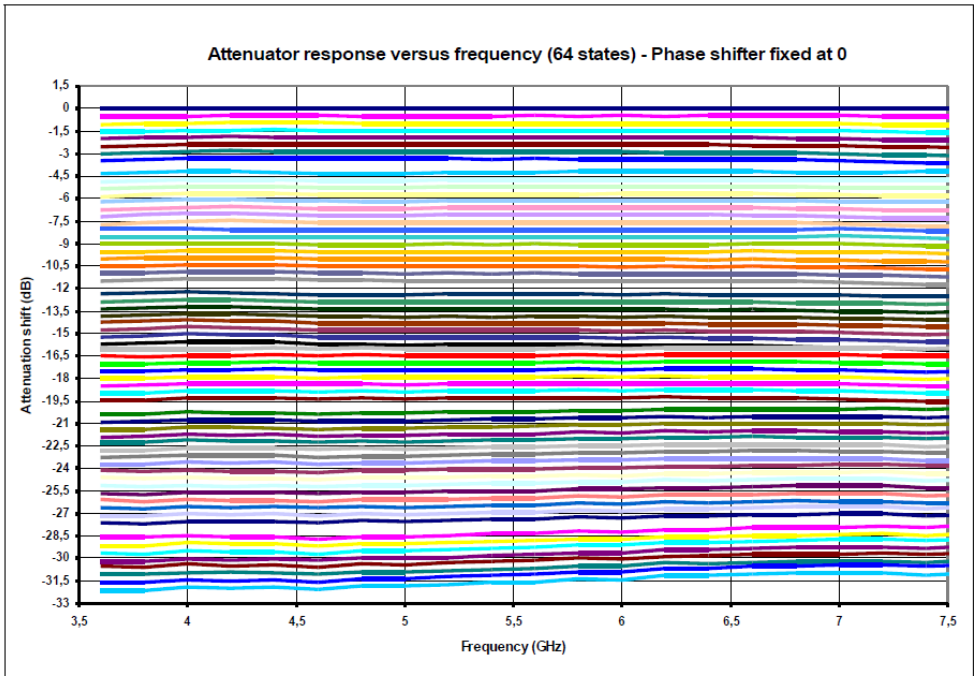

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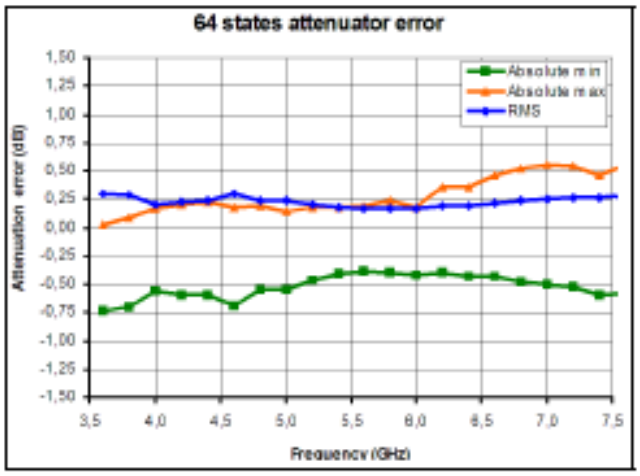


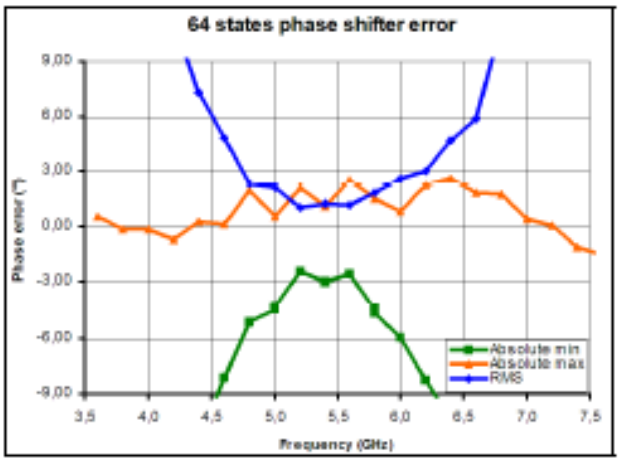


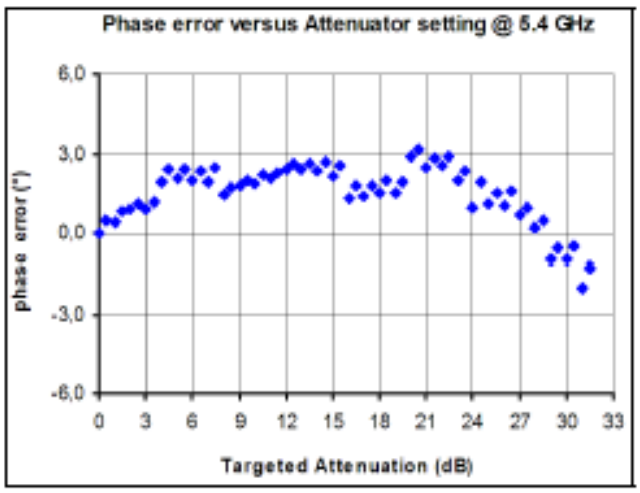


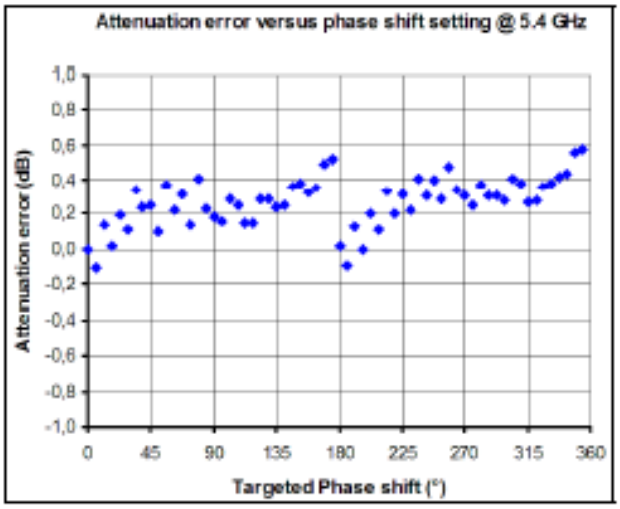


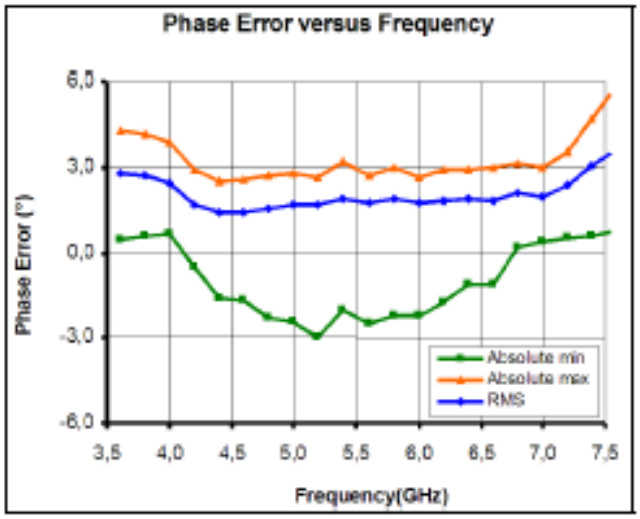


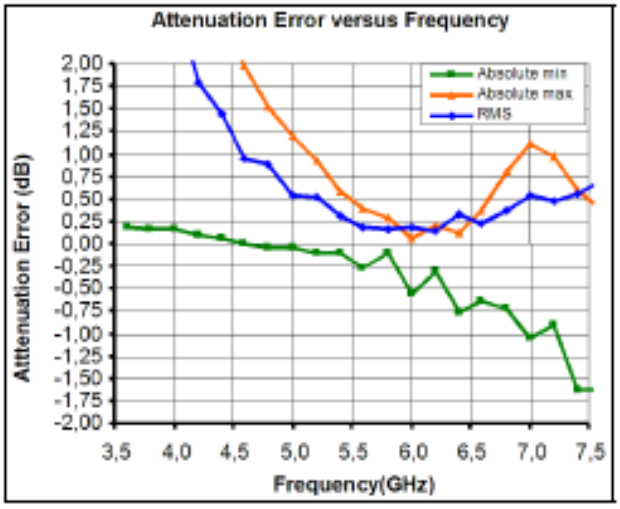

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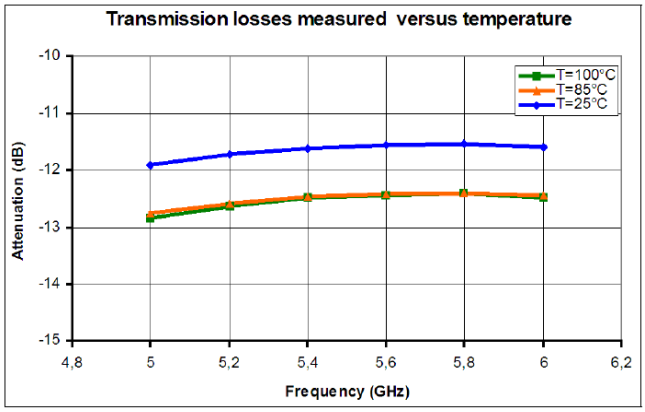
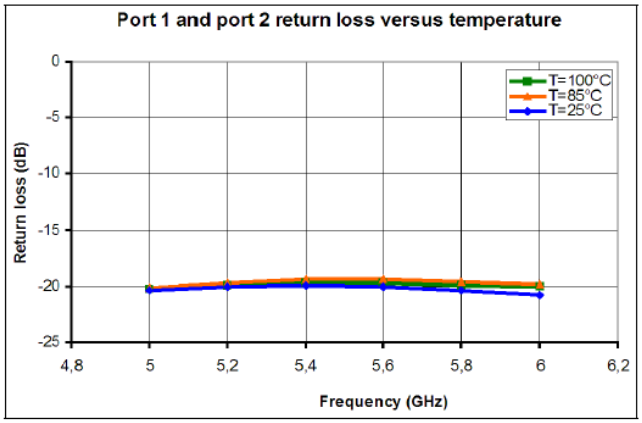
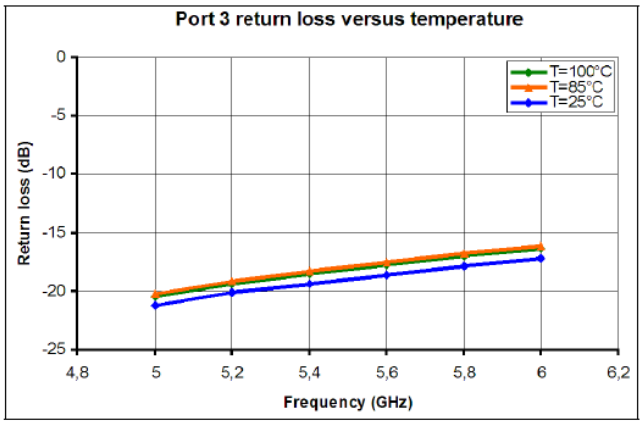


## Logic Truth Table (B0 is loaded first, and B11 last, see timing diagram)

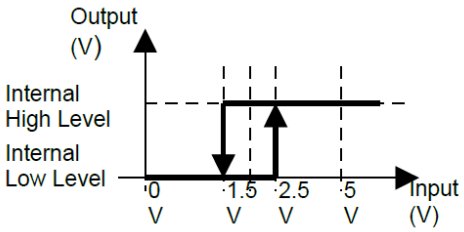
| Bit # | Description | Reference State | Value |
|---|---|---|---|
| B0 (LSB ph) | Phase Shifter B0 | High | 5.625° |
| B1 | Phase Shifter B1 | High | 11.25° |
| B2 | Phase Shifter B2 | High | 22.5° |
| B3 | Phase Shifter B3 | High | 45° |
| B4 | Phase Shifter B4 | High | 90° |
| B5 | Phase Shifter B5 | High | 180° |
| B6 (LSB att) | Attenuator B0 | High | 0.5 dB |
| B7 | Attenuator B1 | High | 1 dB |
| B8 | Attenuator B2 | High | 2 dB |
| B9 | Attenuator B3 | High | 4 dB |
| B10 | Attenuator B4 | High | 8 dB |
| B11 | Attenuator B5 | High | 16 dB |
| CLK | Clock | — | — |
| LE | Latch Enable | — | — |
| SW1 | Not Used | Connected to Ground | — |
| SW2 | Port 1 to Port 2 Switch | High | RF Path between Port 1 & Port 3<br>Port 2 isolated & loaded by 50 Ω |
| | | Low | RF Path between Port 2 & Port 3<br>Port 1 isolated & loaded by 50 Ω |

## Control Logic (CMOS Standard Logic)

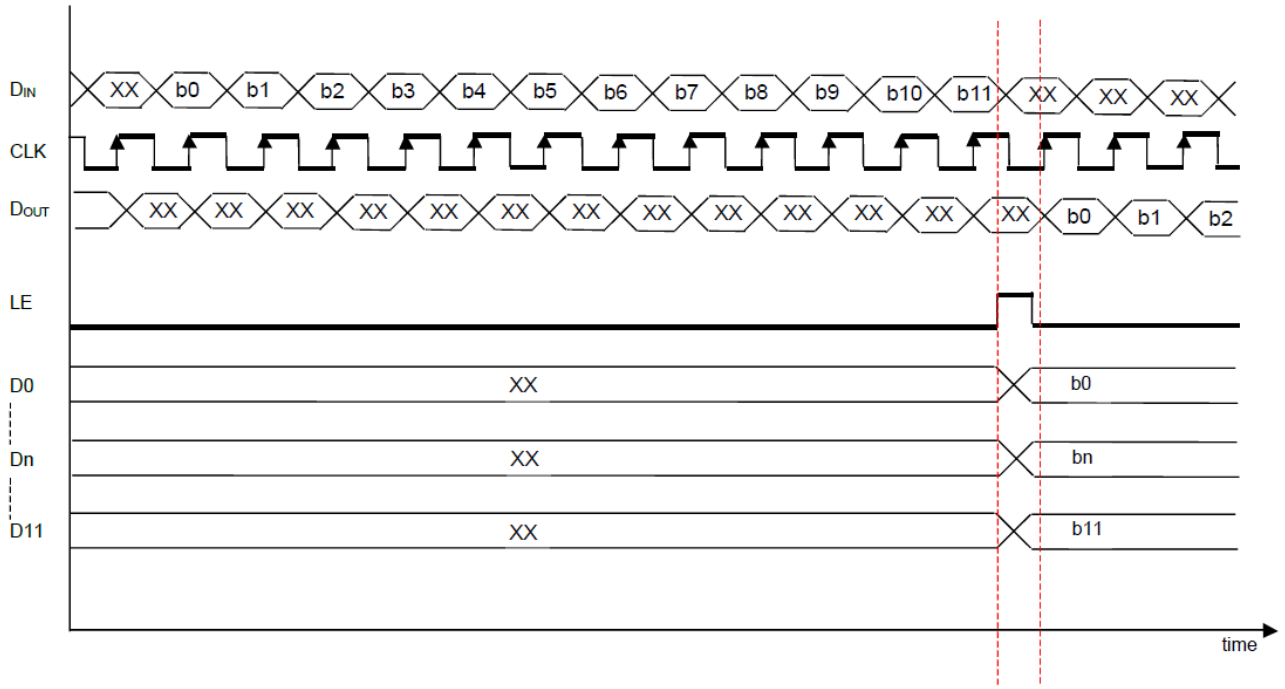
| State | Min. | Max. |
|---|---|---|
| Low | 0 V | 0.2 V x $V_{DD}$ |
| High | 0.5 V x $V_{DD}$ | $V_{DD}$ |

## Input Schmidt Trigger

All inputs (DATA (DIN), Clock (CLK), Latch Enable (LE) and Switch Control (SW2) ) include Schmidt triggers allowing an optimal data transfer to the CGY2175AUH even in a noisy environment and/or high speed data stream.

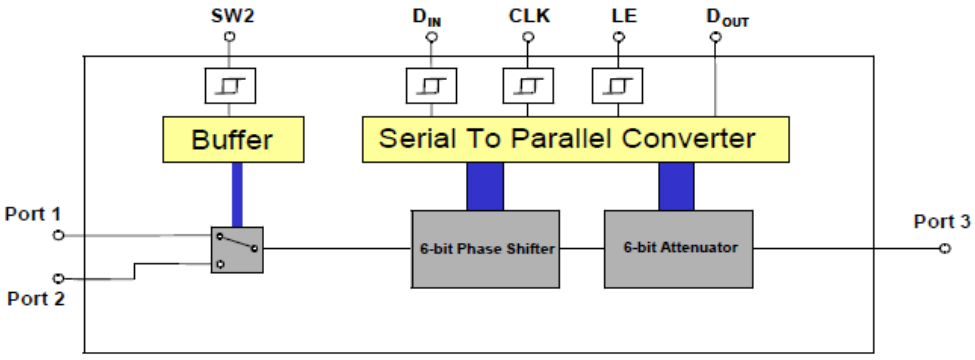


## Timing Diagram




- DATA (DIN) is sampled at the rising edge of the Clock (CLK).
- Latch Enable (LE) must occur after all the 12 bits are loaded (i.e. after the rising edge associated with the bit b11) but before the subsequent rising edge of the Clock.
- The transferred data (DOUT) is available on the rising edge of the Clock following the Latch enable.

$D_{IN}$ is the serial word containing 12 bits of information b0 to b11. Bits D0 to D11 are the internal parallel data used for the digital attenuator and digital phase shifter settings and is formed from the serial word b0 to b11.



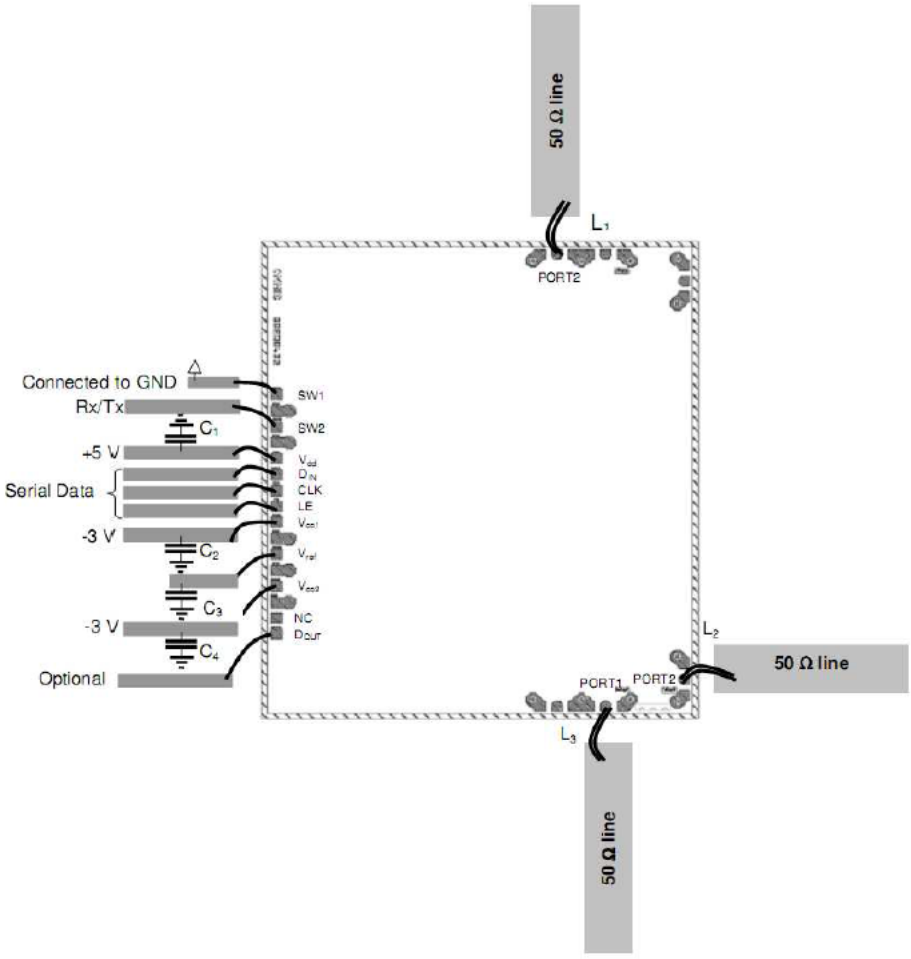

Block Diagram of the CGY2175AUH fully Integrated C-band 3-port T/R chip

## Pad Position[5]

| Pad Name | Coordinate | | Description |
|---|---|---|---|
| | X | Y | |
| SW1 | 80 | 3000 | Not used – Must be connected to ground |
| SW2 | 80 | 2700 | Tx/Rx mode switch command |
| DATA (DIN) | 80 | 2250 | Serial data input |
| CLK | 80 | 2100 | Clock for serial to parallel converter |
| LE | 80 | 1950 | Latch Enable command to load the data |
| DOUT | 80 | 750 | Serial to parallel converter output for testing or to chain several chips |
| Vdd | 80 | 2400 | Schmidt trigger positive supply voltage (+5 V) |
| Vcc1 | 80 | 1800 | Schmidt trigger negative supply voltage (-3 V) |
| Vcc2 | 80 | 1200 | Serial to parallel converter negative supply voltage (-3 V) |
| Vref | 80 | 1500 | Internal voltage supply for Converter – Must be decoupled using 100 nF Nominal value = -2 V |
| Port 1 | 2945 | 70 | RF Input/Output |
| Port 2 | 3625 | 326 | RF Input/Output |
| Port 3 | 2520 | 4325 | RF Input/Output |

5. X = 0, Y = 0 at bottom left corner.

## Bonding Diagram & Assembly Information

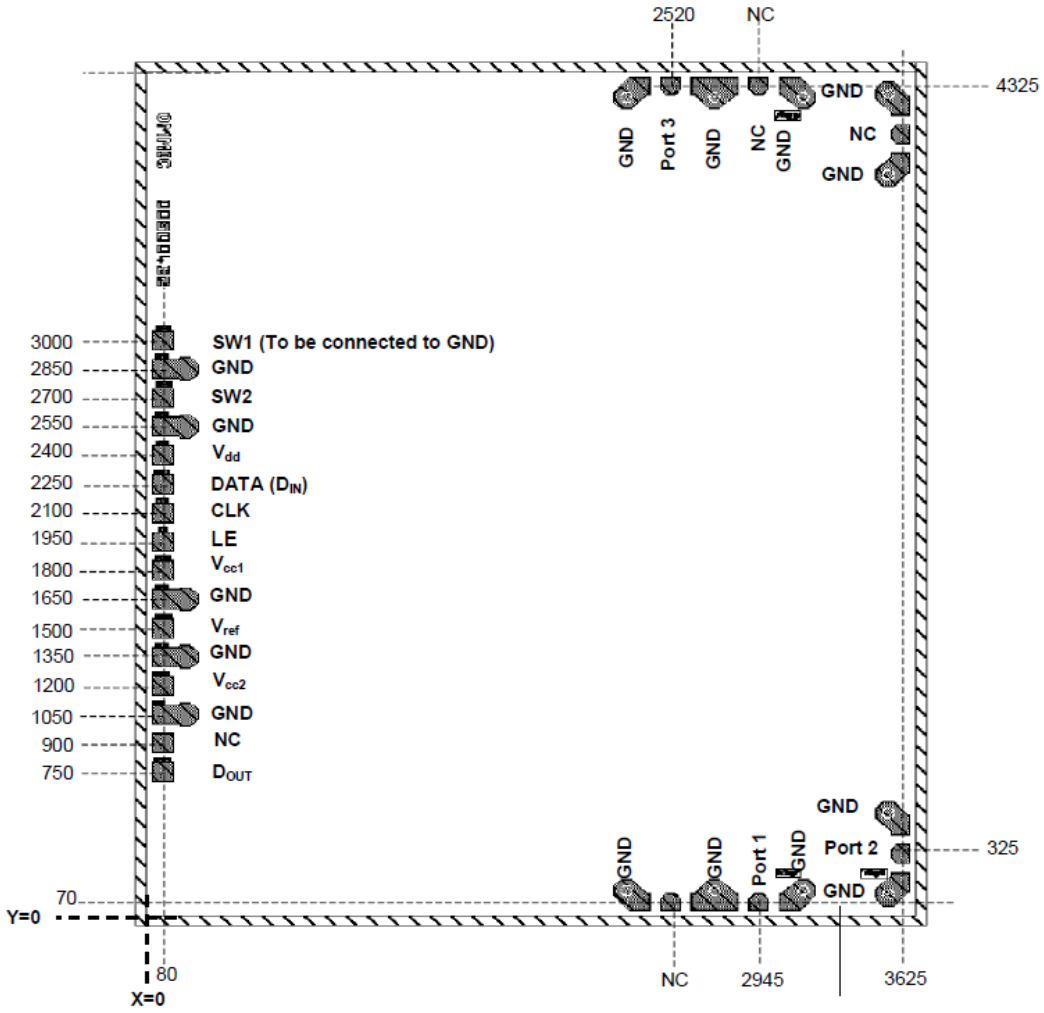



The number of wire bonds to the RF pads (L1, L2, L3) may be doubled to reduce the equivalent inductance. The optimal inductance is 0.35 nH in order to achieve the best return loss in the 5-6 GHz frequency band.

C1, C2, C3, C4 are 100 nF decoupling capacitors.

The pad « SW1 » is not used and should be connected to ground.

## Mechanical Information




Chip Size = 3765 x 4465 µm (before wafer sawing)
DC Pads = 100 x 140 µm, spacing = 150 µm, top metal = Au
RF Pads = 100 x 100 µm, pitch = 150 µm, top metal = Au
Chip Thickness = 100 µm
Backside Metal = TiAu