3-Port, C-Band Integrated Core Chip
4.5 - 6.5 GHz

CGY2175AHV/C1
Rev. V1

Features

- Insertion Loss: 12 dB @ 5.5 GHz
- Phase Shift Range: 360°
- Attenuation Range: 31.5 dB
- RMS Phase Error: 2.0° @ 5.5 GHz
- RMS Amplitude Error: 0.5 dB @ 5.5 GHz
- Total Power Consumption: 0.1 W
- QFN Size: 7 x 7 mm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- RoHS* Compliant

Applications

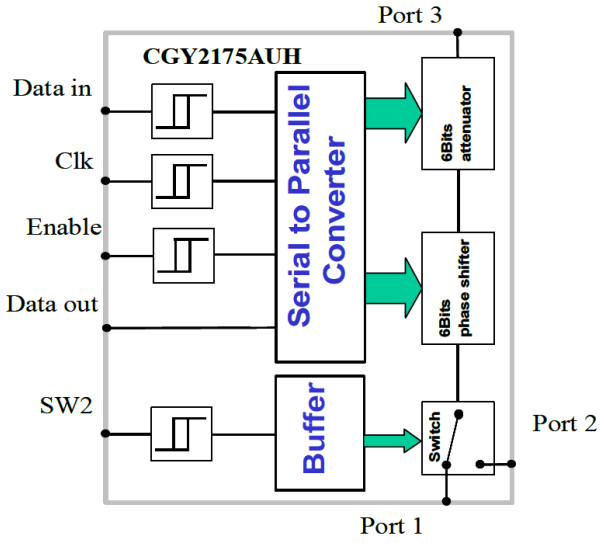
- Radar
- Telecommunication
- Instrumentation

Description

The CGY2175AHV/C1 is a high performance QFN packaged 3 port, 6-bit core chip operating in C-band. It includes a 6-bit phase shifter, a 6-bit attenuator and a T/R switch. The serial to parallel converter minimizes the number of bonding pads and greatly simplifies the use of the core chip functions.

The die is manufactured using 0.18 µm gate length pHEMT Technology. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency. The device is available in a 7x7 mm² 44 leads QFN package.

Block Diagram



Ordering Information

Part Number	Package
CGY2175AHV/C1	

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 5.6 GHz, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	Positive Negative Digital Negative	V	+4.50 -3.25 -3.25	+5.00 -3.00 -3.00	+5.50 -2.75 -2.75
Supply Current	Positive Negative Digital Negative	mA	—	15 20 20	—
Insertion Loss	No Attenuation	dB	—	12	—
Input Return Loss	Port 1 & Port 2	dB	—	-15	-10
Output Return Loss	Port 3	dB	—	-15	-10
Attenuation	Port 1 to Port 3 Port 2 to Port 3	dB	—	12 12	—
Switch Isolation	Port 2 to Port 1	dB	—	TBD	—
Attenuation Range	—	dB	—	31.5	—
RMS Attenuation Error[1,2]	—	dB	—	0.2	—
Attenuation Variation	—	dB	-0.7	—	+0.5
Phase Range	—	°	—	360	—
RMS Phase Error[1,2]	—	°	—	2	—
Phase Variation	—	°	-4	—	+4
P1dB	No Attenuation	dBm	—	20	—
Switching Time	Rx/Tx	ns	—	10	—
Serial Data Rate	—	MHz	—	100	—

1. The RMS value is the root mean square of the error defined as below:
2. Where x_i is the difference between the measured value and the expected value.

$$x_{\text{rms}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \cdots + x_N^2}{N}}$$

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Supply Voltage Positive Negative Digital Negative	 0 to +6 V -4 to 0 V -4 to 0 V
Digital Data Input	0 to +6 V
Input Power @ RF Port 1 & Port 2	25 dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

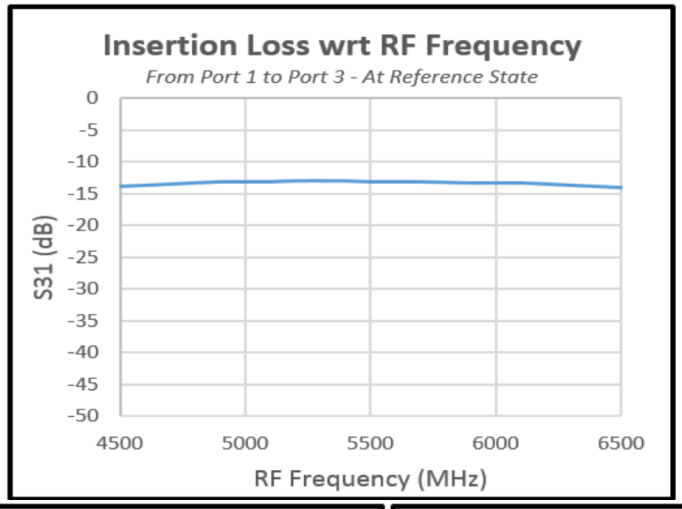
Handling Procedures

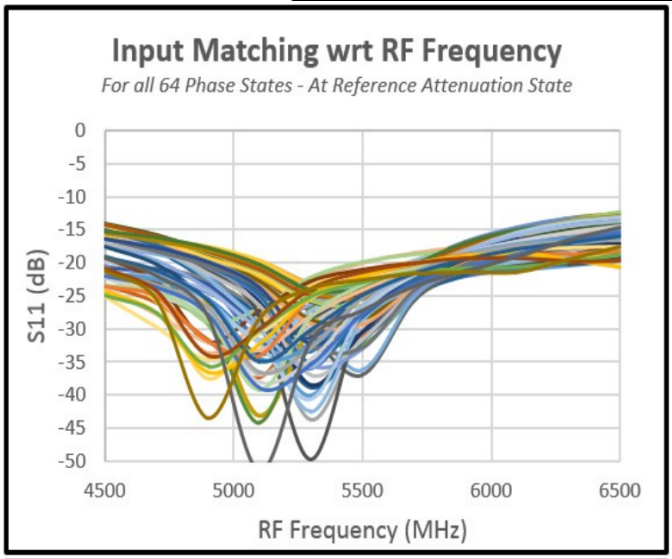
Please observe the following precautions to avoid damage:

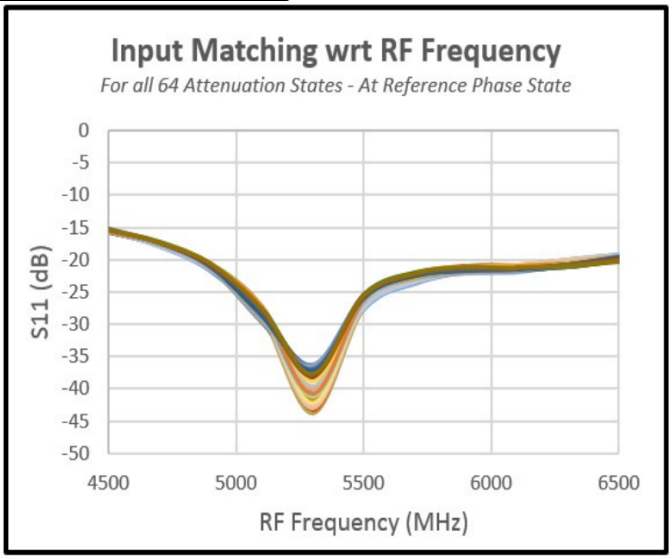
Static Sensitivity

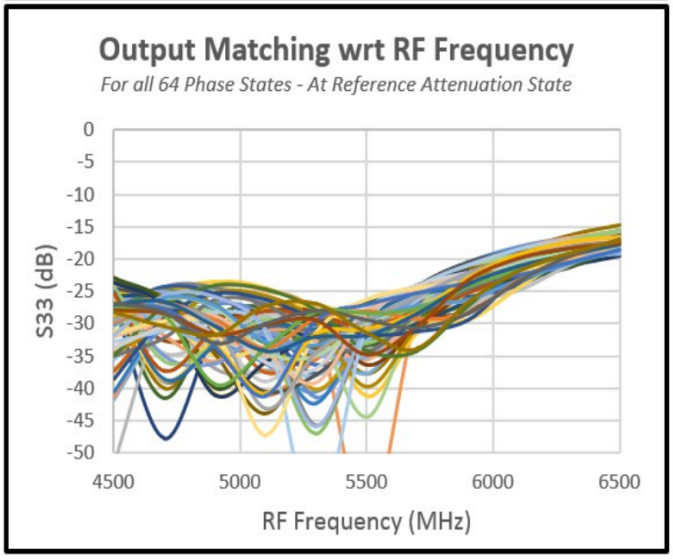
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

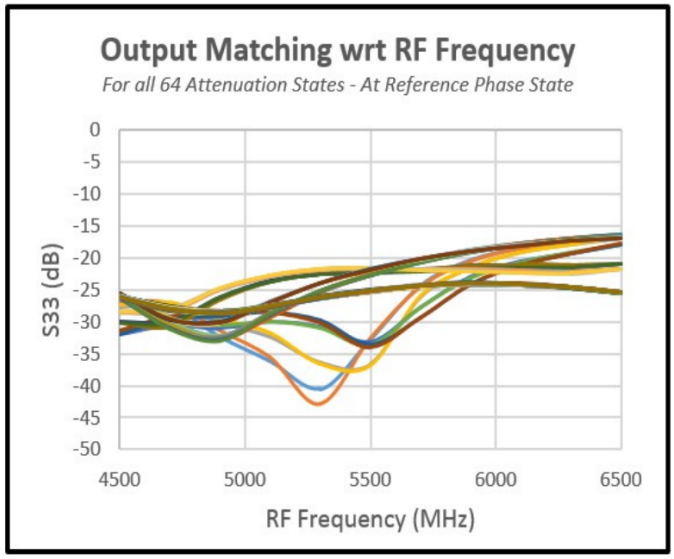
Typical Performance Curves: On Board Measurements



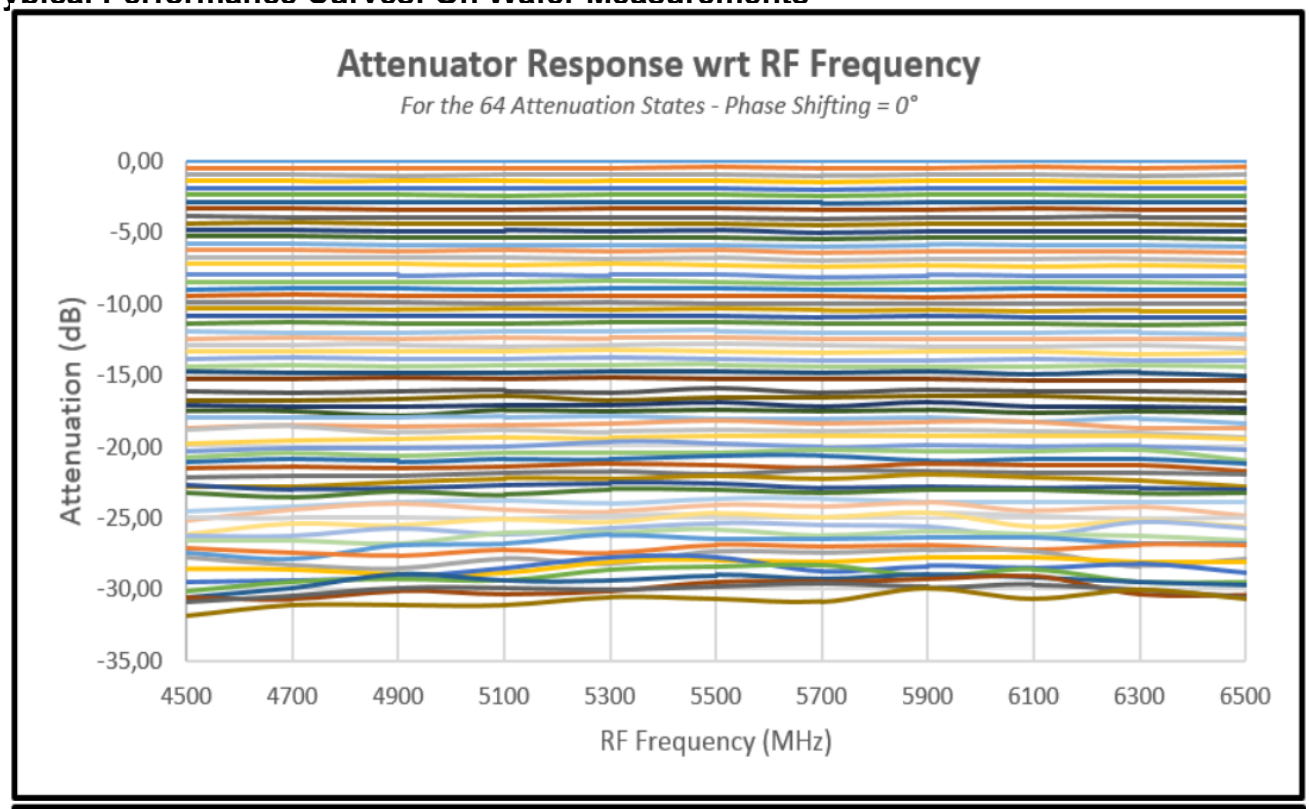


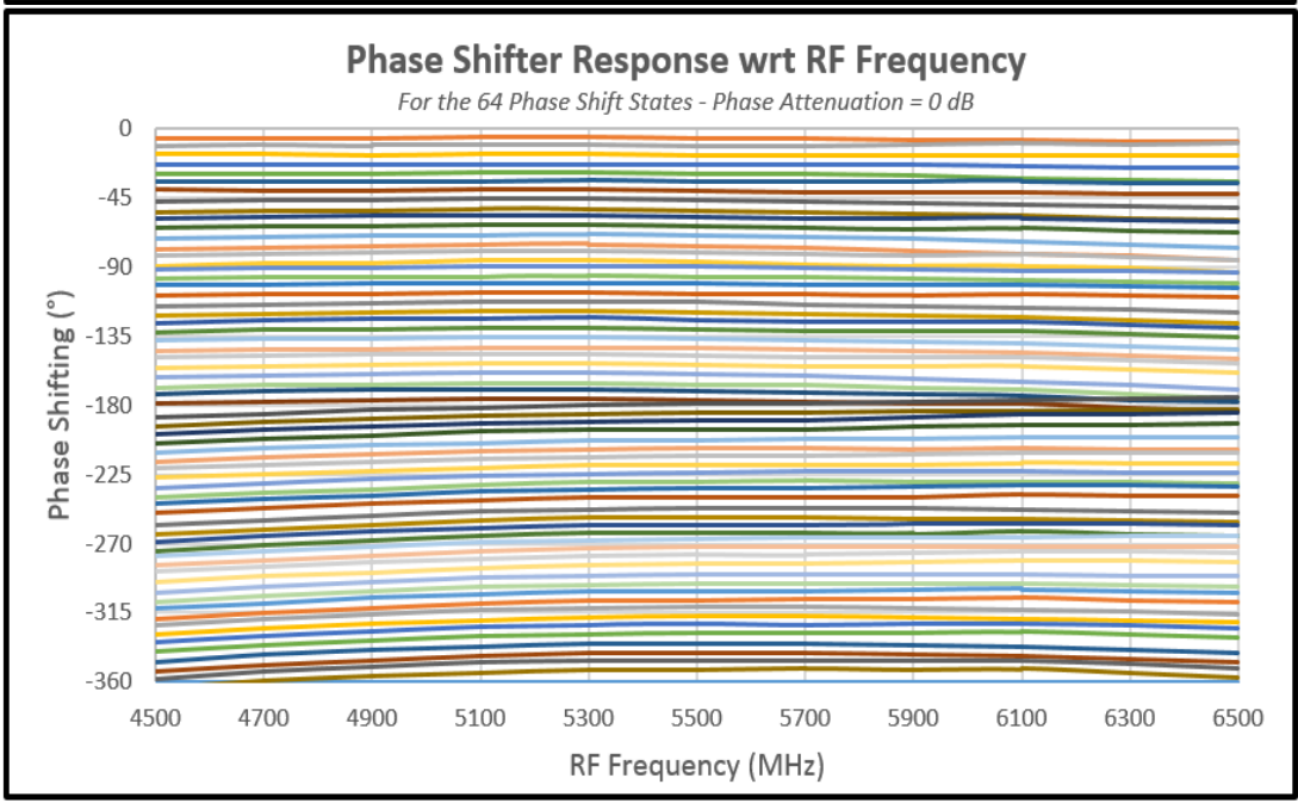




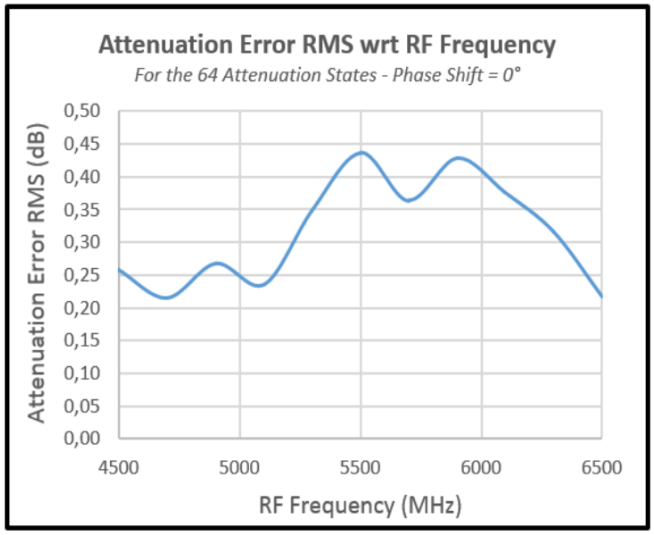


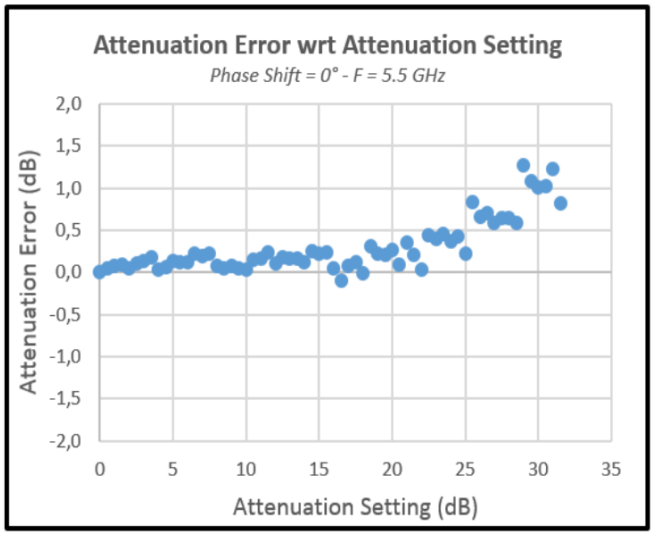
Typical Performance Curves: On Wafer Measurements

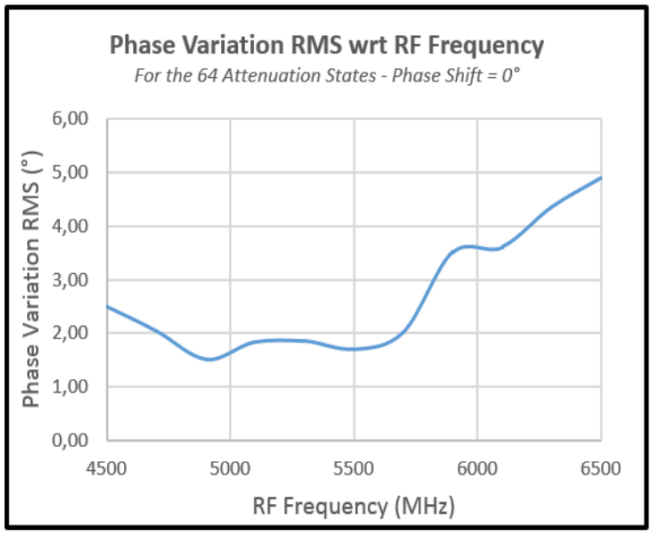


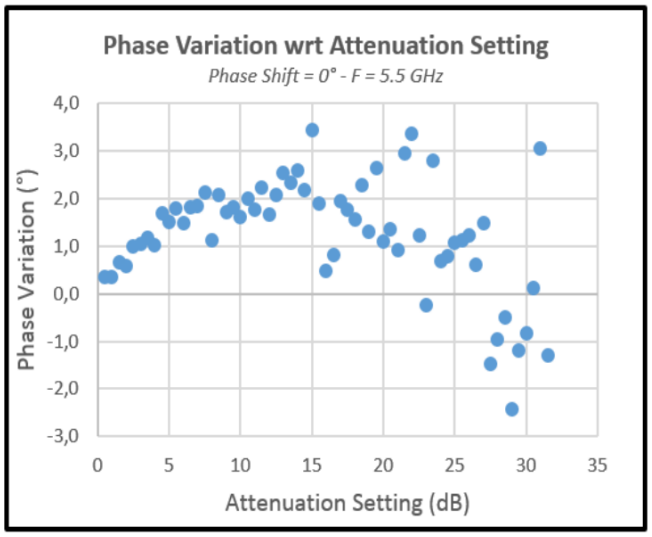


Typical Performance Curves: On Board Measurements









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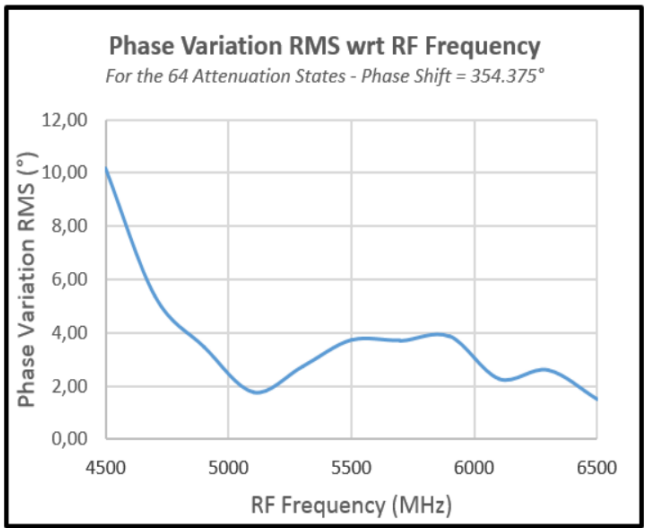

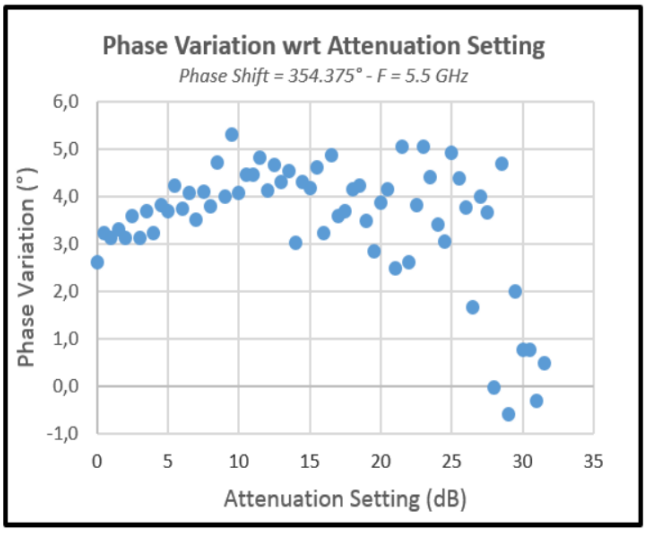

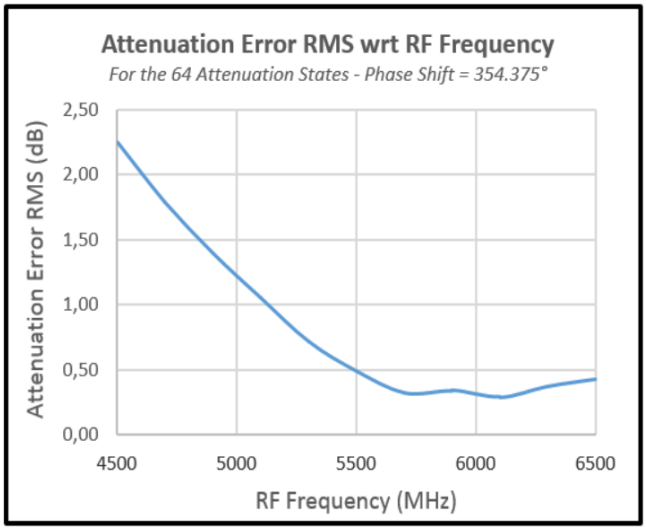

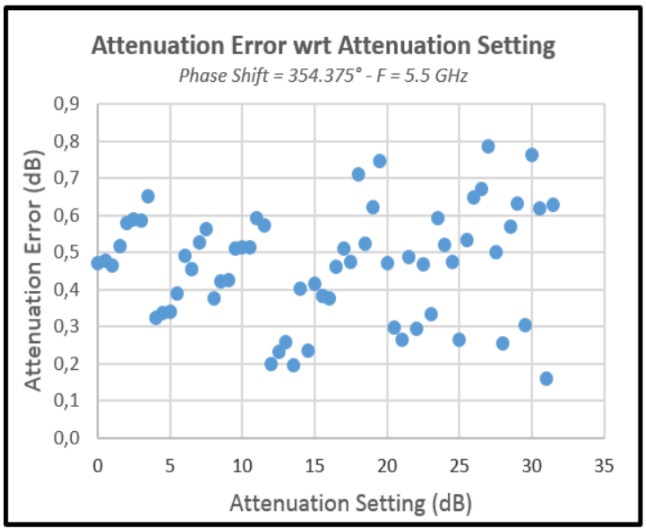

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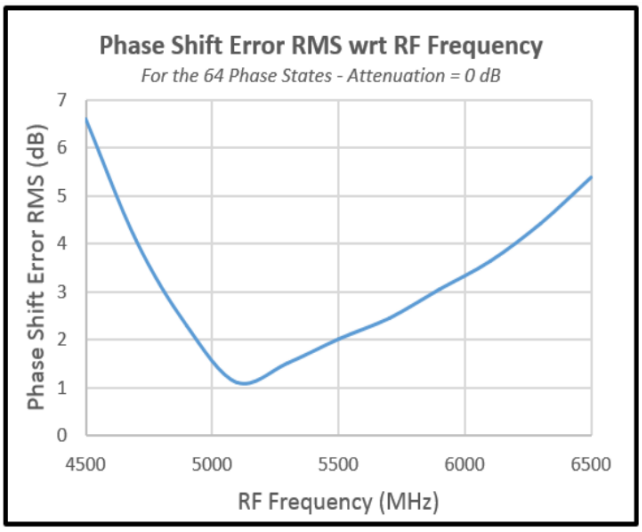

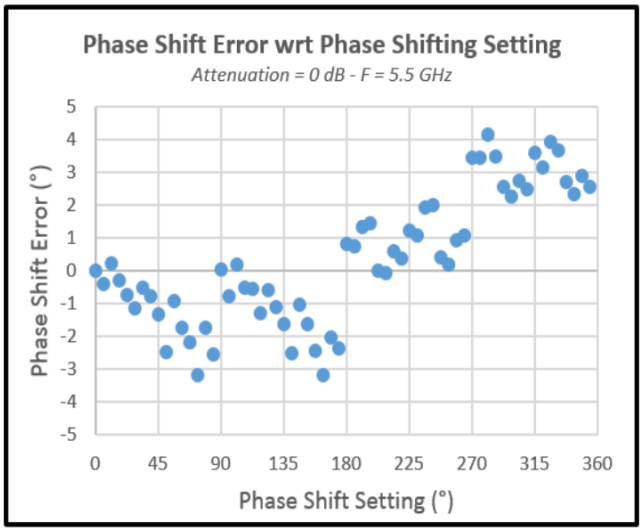

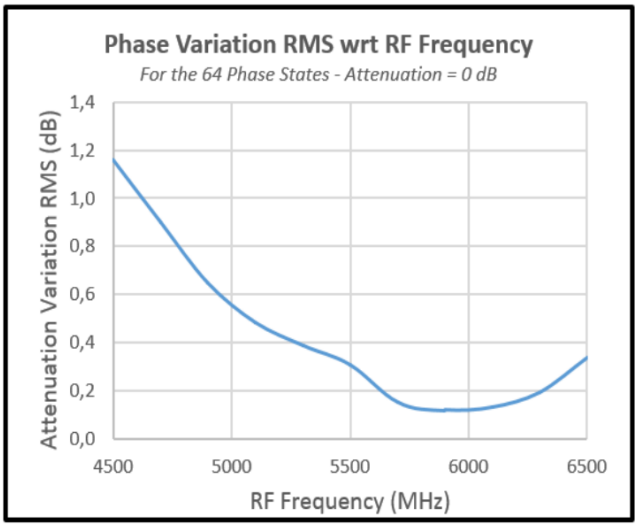

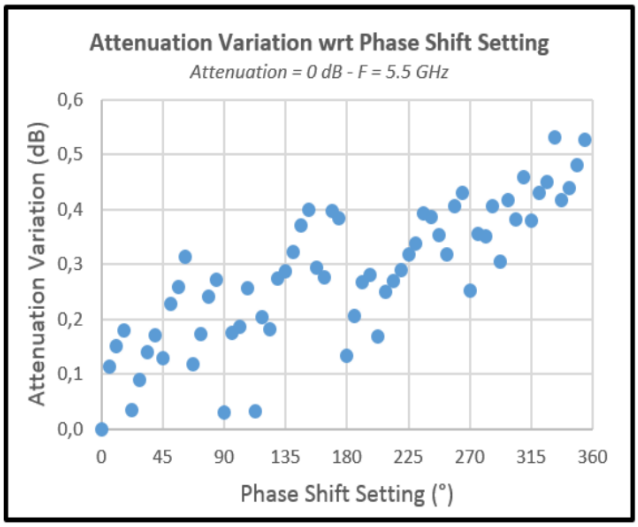

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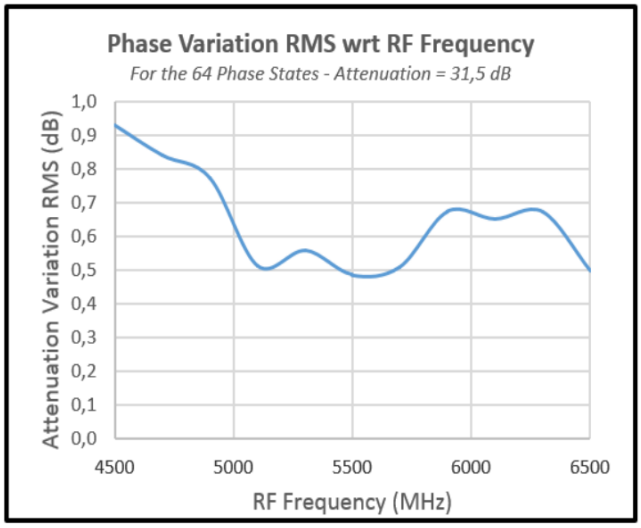

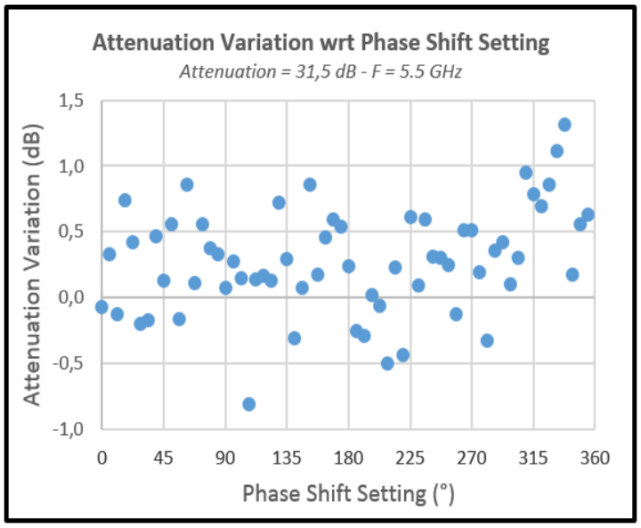

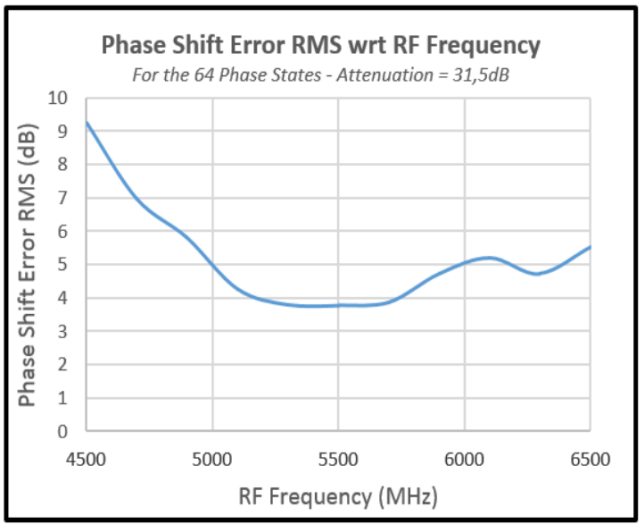

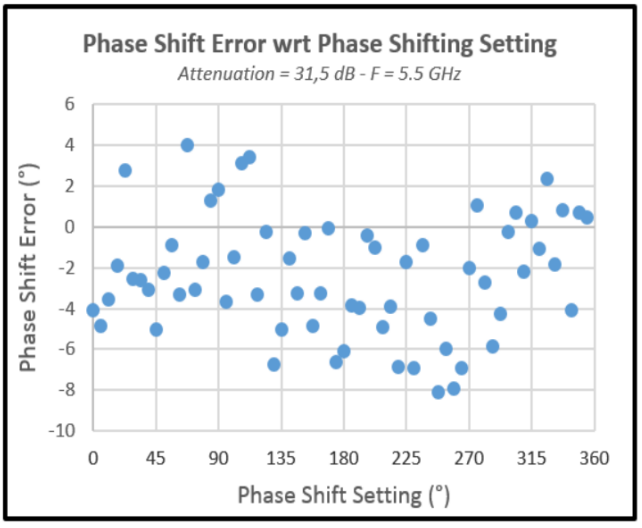

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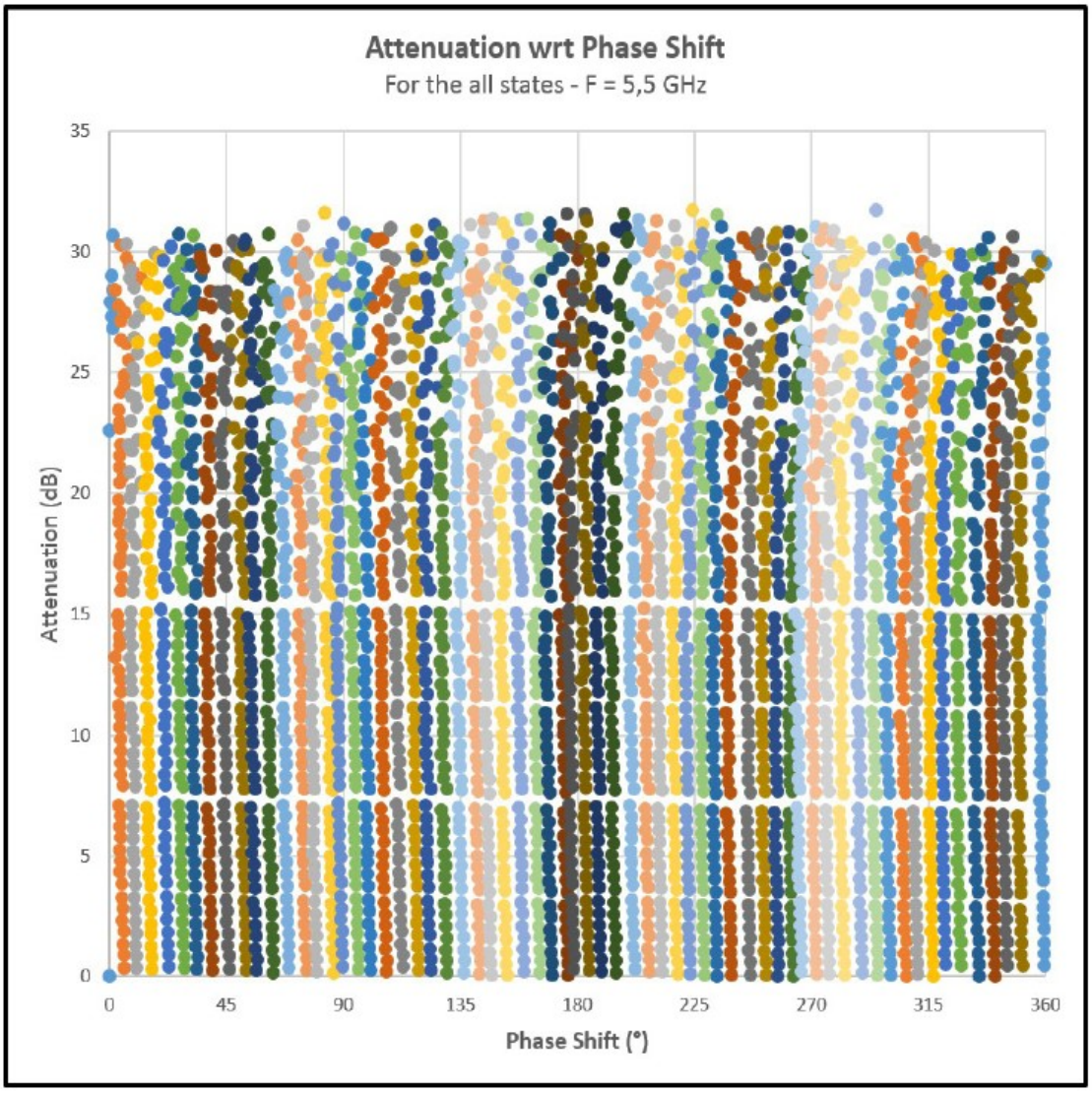


Logic Truth Table (B0 is loaded first, and B11 last, see timing diagram)

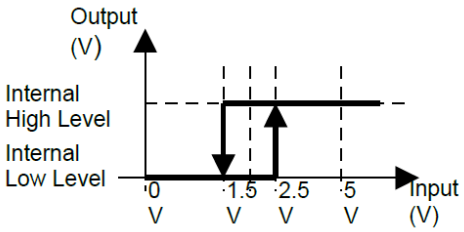
Bit #	Description	Reference State	Value
B0	Phase Shifter B0	High	5.625°
B1	Phase Shifter B1	High	11.25°
B2	Phase Shifter B2	High	22.5°
B3	Phase Shifter B3	High	45°
B4	Phase Shifter B4	High	90°
B5	Phase Shifter B5	High	180°
B6	Attenuator B0	High	0.5 dB
B7	Attenuator B1	High	1 dB
B8	Attenuator B2	High	2 dB
B9	Attenuator B3	High	4 dB
B10	Attenuator B4	High	8 dB
B11	Attenuator B5	High	16 dB
CLK	Clock	—	—
LE	Latch Enable	—	—
SW	Port 1 to Port 2 Switch	High	RF Path between Port 1 & Port 3 Port 2 isolated & loaded by 50 Ω
		Low	RF Path between Port 2 & Port 3 Port 1 isolated & loaded by 50 Ω

Control Logic (CMOS Standard Logic)

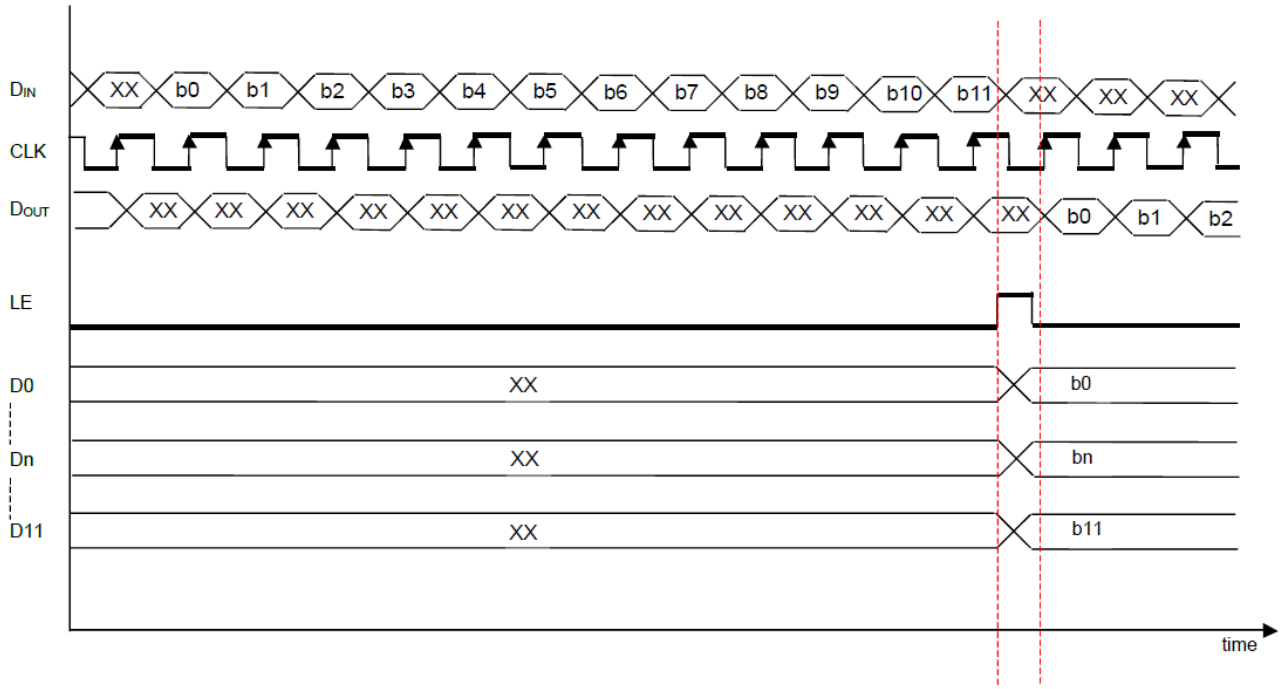
State	Min.	Max.
Low	0	0.2 x V_{DD}
High	0.5 x V_{DD}	V_{DD}

Input Schmidt Trigger

All inputs (DATA (DIN), Clock (CLK), Latch Enable (LE) and Switch Control (SW2)) include Schmidt triggers allowing an optimal data transfer to the CGY2175AHV even in a noisy environment and/or high speed data stream.



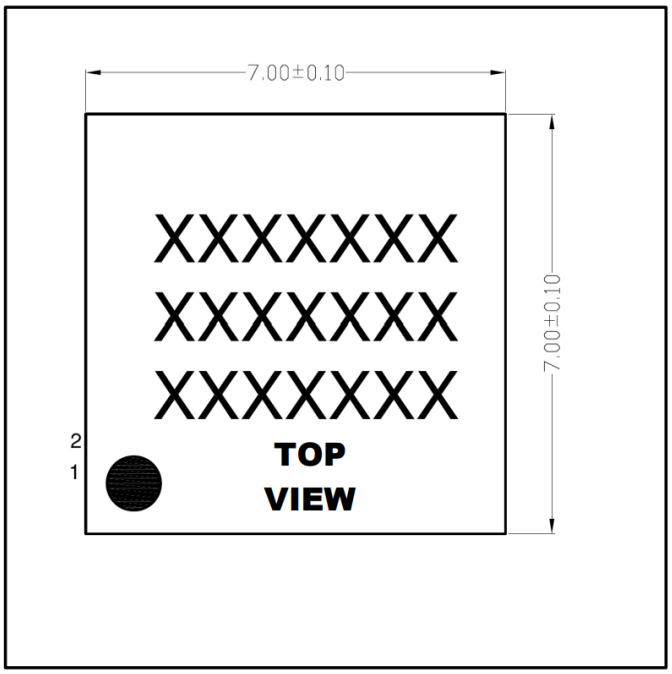
Timing Diagram

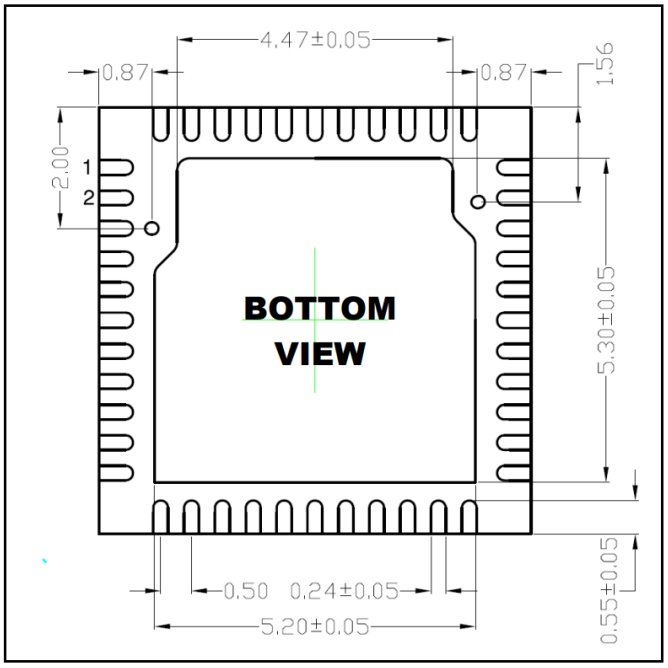


- DATA (DIN) is sampled at the rising edge of the Clock (CLK).
- Latch Enable (LE) must occur after all the 12 bits are loaded (i.e. after the rising edge associated with the bit b11) but before the subsequent rising edge of the Clock.
- The transferred data (DOUT) is available on the rising edge of the Clock following the Latch enable.

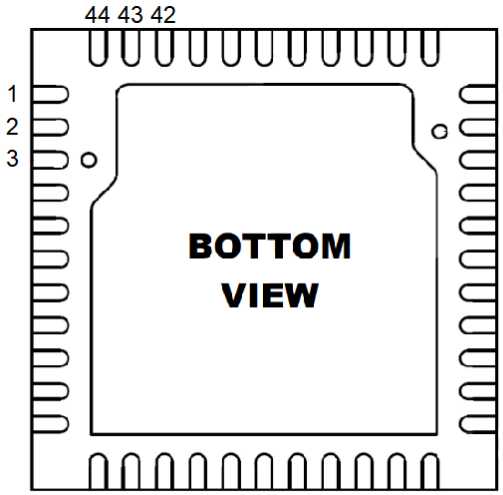
Bits D0 to D11 are the internal parallel data used for the digital attenuator and digital phase shifter settings.

Outline Drawing





Type	Description	Terminals	Pitch (mm)	Package size (mm)
QFN	Quad Flat No lead with exposed heat sin	44	0.5	7 x 7 x 0.90



Pin Configuration

Pin#	Symbol	Description
1, 5 - 11, 23 - 30, 37 - 44	N/C	No Connection
2, 4, 12, 13, 31, 33, 34, 36	GND	Ground
3	RF3	RF Port 3
14	SW	Switch between RF Port1 & RF Port 2
15	VDD	Positive Supply Voltage
17	CLK	Clock Input
16	D_{IN}	Data Input
18	LE	Latch Enable Input
19	VCC1	Negative Supply Voltage
20	VREF	Internal voltage supply for converter (must be decoupled using 100 nF nominal value = -2 V)
21	VCC2	Negative Supply Voltage of Digital Part
22	D_{OUT}	Data Output
32	RF1	RF Port 1
35	RF2	RF Port 2

5. MACOM recommends connecting No Connection (N/C) pins to ground.
6. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.