6-Bit, X-Band Core Chip
8 - 12 GHz

CGY2170YUH/C1
Rev. V2

Features

- Gain Tx/Rx: 6 dB @ 10 GHz
- RMS Phase Error: 3.0° @ 9 - 10 GHz
- RMS Amplitude Error: 0.4 dB @ 8 - 11 GHz
- Output P1dB Tx: 12 dBm
- Output P1dB Rx: 12 dBm
- Return Loss: < -15 dB @ 10 GHz (all states)
- Power Consumption: 0.33 W
- Die Size: 4700 x 3800 x 100 µm
- RoHS* Compliant

Applications

- AESA Radar
- Telecommunication
- Instrumentation

Description

The CGY2170YUH/C1 is a high performance GaAs MMIC T/R 6-bit core chip operating in X-band. The product has three RF ports and includes three switches a 6-bit phase shifter, a 6-bit attenuator, and amplifiers. It has a phase shifting range of 360° and a gain setting range of 31.5 dB. There is also a voltage variable attenuator in between the phase shifter and first amplifier stage for gain control. It covers the frequency range from 8 to 12 GHz and provide 5.8 dB of gain at 10 GHz.

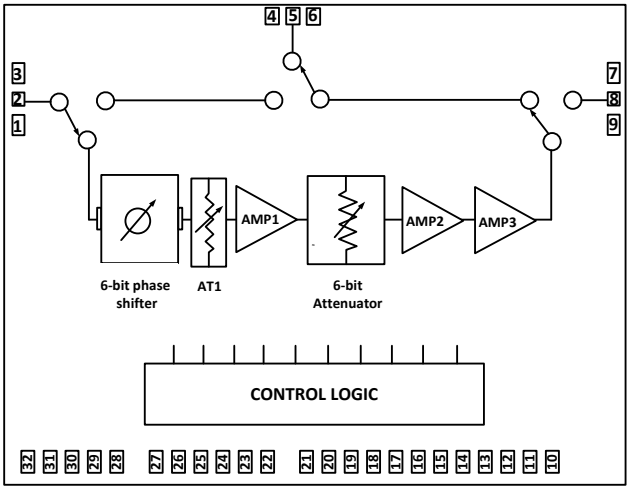
The on-chip control logic with serial input register minimizes the number of control lines and greatly simplifies the control interface of this device.

This die is manufactured using 0.18 µm gate length ED02AH pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability. This technology has been evaluated for space applications and is on the European preferred parts list of the European space agency.

Ordering Information

Part Number	Package
CGY2170YUH/C1	Die
CGY2170YUH/C1/EK	Sample Board

Block Diagram



Pin Configuration

Pin #	Function	Pin #	Function
1	Ground	17	DIN
2	RXin	18	LE
3	Ground	19	CLR
4	Ground	20	VDN
5	COM	21	Ground
6	Ground	22	AT1
7	Ground	23	AT2
8	RXout	24	VSS
9	Ground	25	VG3
10	STBRX	26	VG2
11	STBTX	27	VG1
12	DOUT	28	Ground
13	VSN	29	VD3
14	T/R	30	VD2
15	CS	31	VD1
16	CLK	32	Ground

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Configuration and Functional Description

Pin #	Function	Description
1	Ground	Ground
2	RXin	Rx Input
3	Ground	Ground
4	Ground	Ground
5	COM	COM
6	Ground	Ground
7	Ground	Ground
8	RXout	Rx output
9	Ground	Ground
10	STBRX	For control of external Rx LNA
11	STBTX	For control of external Tx PA
12	DOUT	Data Output
13	VSN	Negative supply voltage
14	T/R	T/R switches control
15	CS	Chip select
16	CLK	Clock Input
17	DIN	Data Input
18	LE	Latch Enable Input
19	CLR	Clear function for register
20	VDN	Positive Supply Voltage
21	Ground	Ground
22	AT1	Input for external control of additional attenuator1
23	AT2	Input for external control of additional attenuator2
24	VSS	Negative Supply Voltage
25	VG3	Gate Voltage Supply 3
26	VG2	Gate Voltage Supply 2
27	VG1	Gate Voltage Supply 1
28	Ground	Ground
29	VD3	Drain Voltage Supply 3
30	VD2	Drain Voltage Supply 2
31	VD1	Drain Voltage Supply 1
32	Ground	Ground

1. STBTX and STBRX should remain open circuit if not required for external amplifier control.

Electrical Specifications: Freq. = 10 GHz (unless otherwise specified), T_A = +25°C, I_{D1} = 20 mA, I_{D2} = 23 mA, I_{D3} = 40 mA, I_{DN} = 2.5 mA, I_{SS} = 4 mA, I_{SN} = 21.5 mA

Parameter	Test Conditions	Units	Min.	Typ.	Max.
VD1[2]	Positive	V	+2.5	+3	+3.5
ID1	Positive	mA	10	20	40
VD2[2]	Positive	V	+2.5	+3	+3.5
ID2	Positive	mA	12	23	50
VD3[2]	Positive	V	+2.5	+3	+3.5
ID3	Positive	mA	20	40	80
VDN[2]	Positive	V	+2.5	+3	+3.5
IDN	Positive	mA	1	2,5	10
VSS[2]	Negative	V	-3.5	-3.0	-2.5
ISS	Positive	mA	1	4	10
VSN[2]	Negative	V	-3.5	-3.0	-2.5
ISN	Positive	mA	10	21,5	30
Gain TX/RX	8 GHz 10 GHz 12 GHz	dB	5.0	5.8 6.0 6.5	7.5
Noise Figure	@ Reference State	dB	—	8	—
Input Return Loss	All States	dB	-20	-15	-12
Isolation	—	dB	35	—	—
Attenuation Range	—	dB	—	31.5	—
RMS Attenuation Error[3]	64 Attenuation States & at Reference Phase State	dB	—	0.4	0.6
Attenuation Variation	64 Phase State & at Reference Attenuation State	dB	—	1.2	1.5
Phase Range	—	°	—	-354	—
RMS Phase Error[3]	64 Phase State & at Reference Attenuation State 8 GHz 9 - 11 GHz 8 - 12 GHz	°	—	 3 4	 4.5 4 5
Phase Variation	64 Attenuation States & at Reference Phase State 0 - 24 dB 24 - 31.5 dB	°	—	—	 ±5 ±8
Output P1dB (TX/RX)	—	dBm	11	13	—
Internal attenuation (AT1)[4]	Supplied by negative voltage from -3 to 0 V	dB	—	2	—
Switching Time	—	ns	—	30	—
Serial Data Rate	—	Mbps	—	20	>230

2. V_{D1}, V_{D2}, V_{D3} and V_{DN} can be biased together, V_{SS} and V_{SN} can also be biased together.
3. The RMS value is the root mean square of the error defined as below:

$$x_{RMS} = \sqrt{\frac{1}{N}\sum_{i=0}^{N} x_i^2} = \sqrt{\bar{x}_i^2 + \sigma_{x_i}^2}$$

Where x_i is the difference between the measured value and the theoretical value, x_i is the mean value of the N x_i, and σxi is the stand and deviation of x_i.

4. To compensate process variation, one variable attenuator is inserted between phase-shifter and first amplifier. A gain adjustment is obtained with an analog voltage applied on 1 additional PAD:AT1, Min and Max Gain Spec guaranteed at AT1 = 0 V & AT1 = -3 V respectively.

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Supply Voltage VDN, Positive VSN, Negative VSS, Digital Negative VD1,VD2,VD3 Drain	 -1 to +5 V -5 to +1 V -6 to 0 V 0 to +6 V
Digital Data Input	-1 to +7 V
Input Power	25 dBm
Junction Temperature[7]	+150°C
Operating Temperature[8]	-40°C to +85°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq +150°C$ will ensure MTTF > 1 x 10^{11} hours.
8. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 42°C/W @T_{amb}=+25°C.
   a) For T_C = +25°C,
   T_J = 39°C @3 V, 110 mA
   b) For T_C = +85°C,
   T_J = 101°C @3 V, (Θjc) = 49°C/W

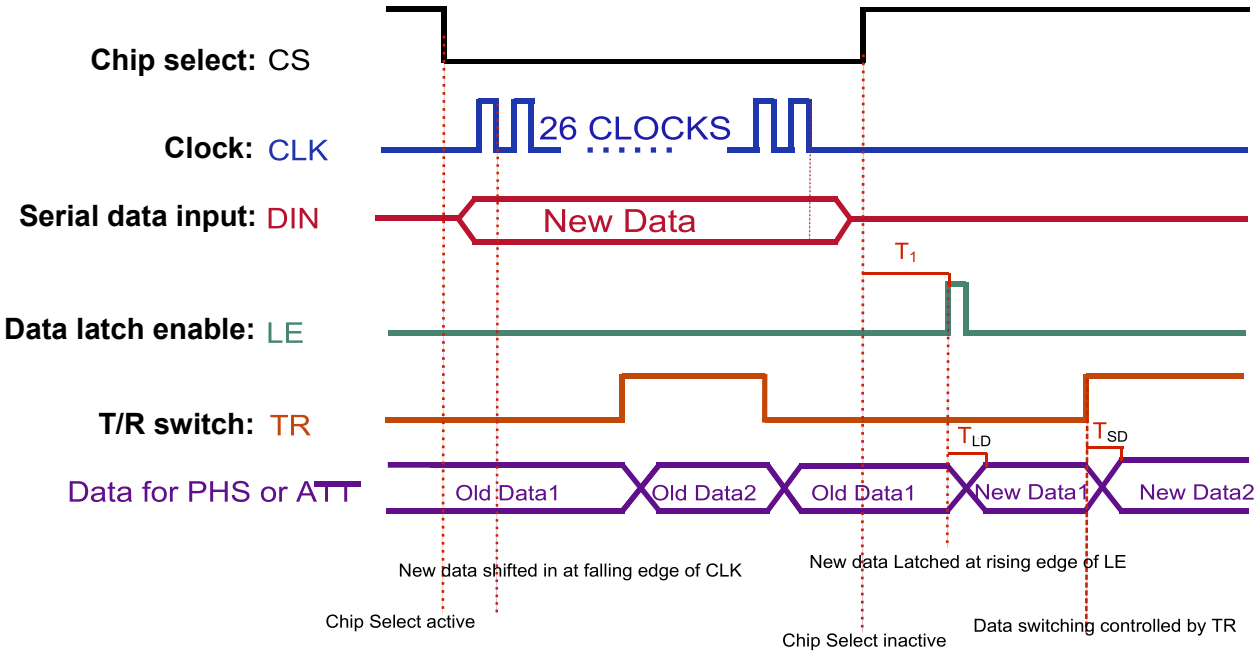
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Timing Diagram



- The serial data input is controlled by falling edge of signal CLK and will be shifted into a 26-bit shift register and will be latched on LE rising edge and complete data update.

- The control data during transmit and receive are saved in two independent latches. Under the control of the T/R switches control, the control data will control phase shifter and attenuator with Time Division Multiplexing (TDM).
  new data 1: SR1 to SR6 for Phase; ATR1 to ATR6 for Attenuation (T/R="0",in Rx mode).
  new data 2: ST1 to ST6 for PHS Phase; ATT1 to ATT6 for Attenuation (T/R="1",in Tx mode).
  The delay time [t1] is defined by the user.
  [T_{SD}] : Tx/Rx switching time
  [T_{LD}] : data latching time

- The serial register clear function CLR is active at low level.

Control Voltage (Standard Logic)

State	V Min.	V Max.
Low	0 V	1 V
High	2.5 V	V_{DN}

Switching Control() T/R

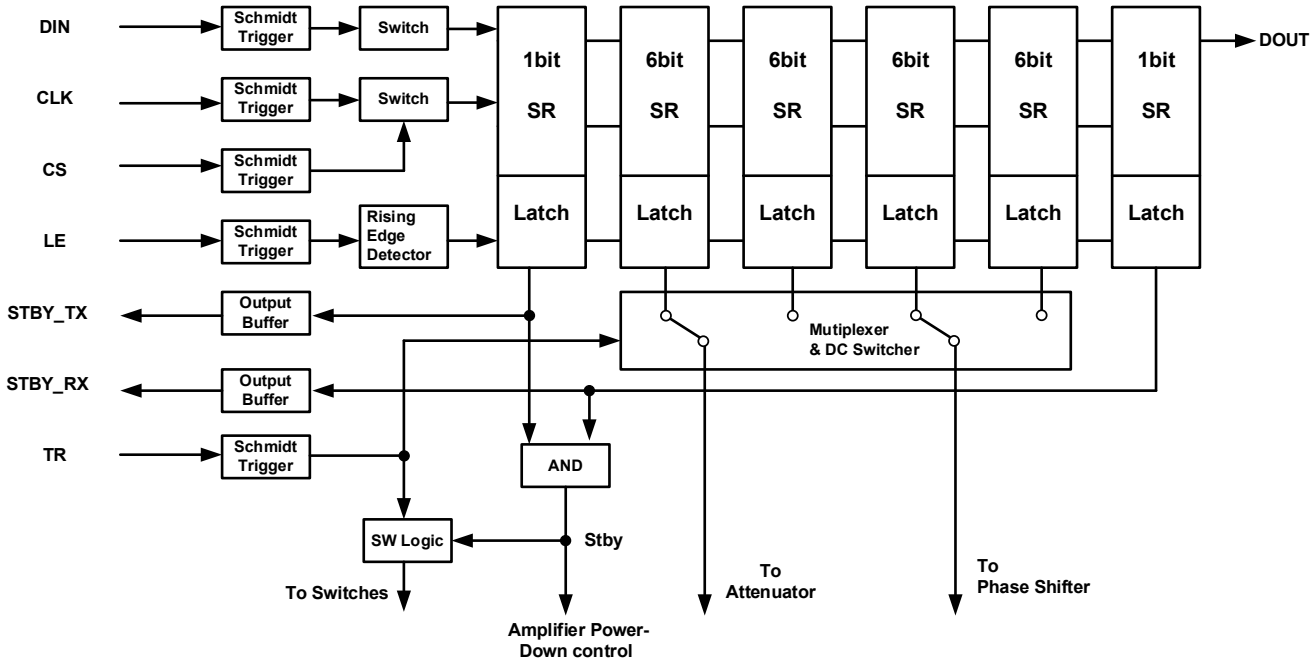
T/R Voltage	Switches Mode
Low (0 V)	RX
High (3 V)	TX

Control Word Definition (active State HIGH)[9]

Bit #	Name	Reference State	Active state	Value	Description
B0	SD0	Low	High	Standby for Rx	ST_RX
B1	ST1	Low	High	5.625°	TX Phase
B2	ST2	Low	High	11.25°	
B3	ST3	Low	High	22.5°	
B4	ST4	Low	High	45°	
B5	ST5	Low	High	90°	
B6	ST6	Low	High	180°	
B7	SR1	Low	High	5.625°	RX Phase
B8	SR2	Low	High	11.25°	
B9	SR3	Low	High	22.5°	
B10	SR4	Low	High	45°	
B11	SR5	Low	High	90°	
B12	SR6	Low	High	180°	
B13	ATT1	Low	High	0.5 dB	TX Attenuation
B14	ATT2	Low	High	1 dB	
B15	ATT3	Low	High	2 dB	
B16	ATT4	Low	High	4 dB	
B17	ATT5	Low	High	8 dB	
B18	ATT6	Low	High	16 dB	
B19	ATR1	Low	High	0.5 dB	RX Attenuation
B20	ATR2	Low	High	1 dB	
B21	ATR3	Low	High	2 dB	
B22	ATR4	Low	High	4 dB	
B23	ATR5	Low	High	8 dB	
B24	ATR6	Low	High	16 dB	
B25	SD1	Low	High	Standby for Tx	ST_TX

9. Power-on state all bits at 0, including B0 & B25.

Serial to Parallel Converter Block Diagram[10,11]



10. The RX or TX modes (state of the switches) are only set by TR PAD.
The T/R PAD selects also which set of control bits (RX or TX) are routed to the phase-shifter and attenuator controls.

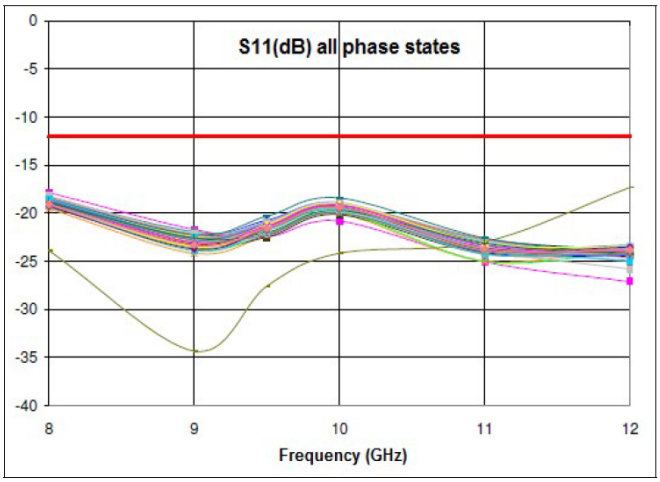
11. The stand-by bits ST0 & ST25 have no effect on the circuit individually , only when both are set to 1 , the amplifiers go in low power mode.
There is no need to set ST0 or ST25 alone to '1' , unless the Output PADS ST_RX or ST_TX are used to control external amplifiers.

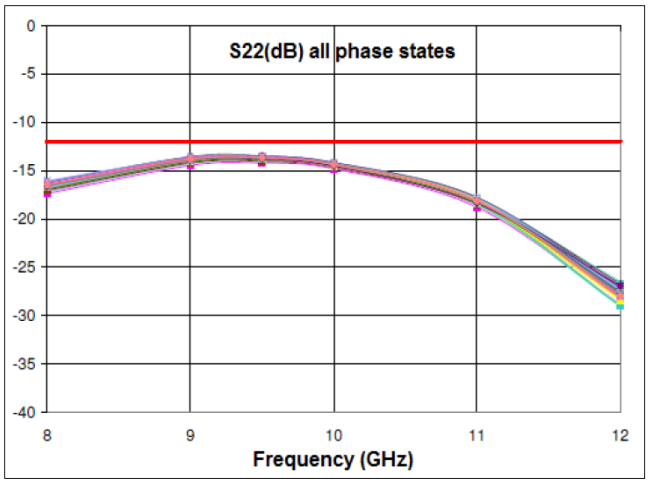
Serial Interface Timing Characteristics

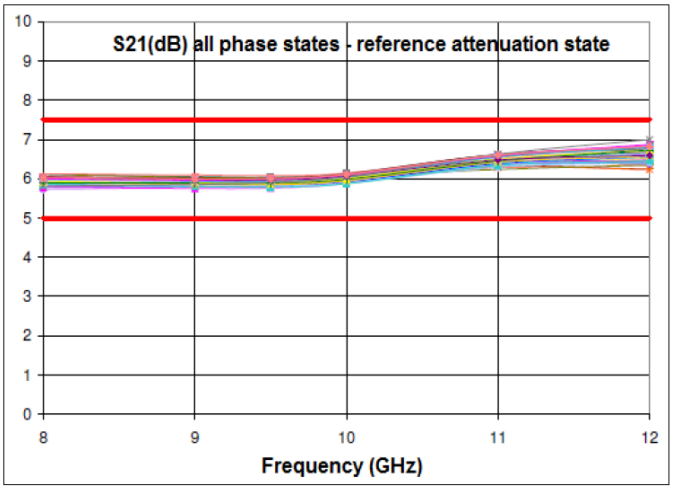
Parameter	Typical	Unit
Maximum Clock Rate	100	MHz
Minimum Clock Period	10	ns
Minimum Pulse Width High	2	ns
Minimum Pulse Width Low	2	ns
Setup Time, CS to CLK	2	ns
Hold Time, CLK to CS	2	ns
Setup Time, DIN to CLK	2	ns
Hold Time, CLK to DIN	2	ns
Minimum Time, CS to LE (T_1)	2	ns
LE to DIN Rise Time (t_{LD})	2	ns
TR to Transmit data RiseTime (t_{SD})	50	ns
TR to Receive data Fall Time	50	ns

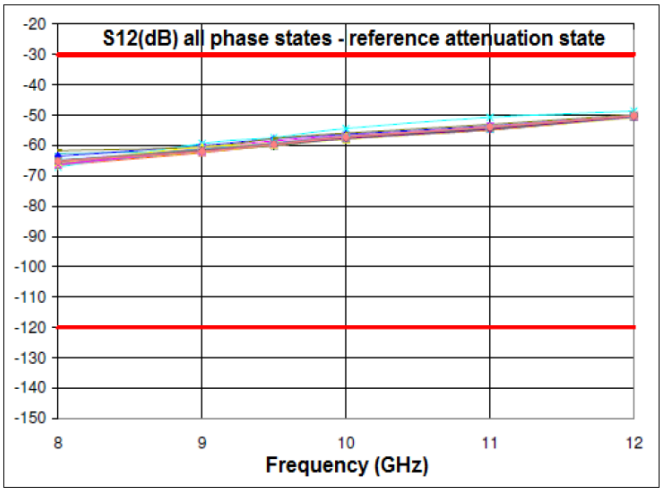
Typical Performance Curves: On Wafer Measurements

Calculated with input and output inductance of 0.5 nH to take into account the bond inductance.









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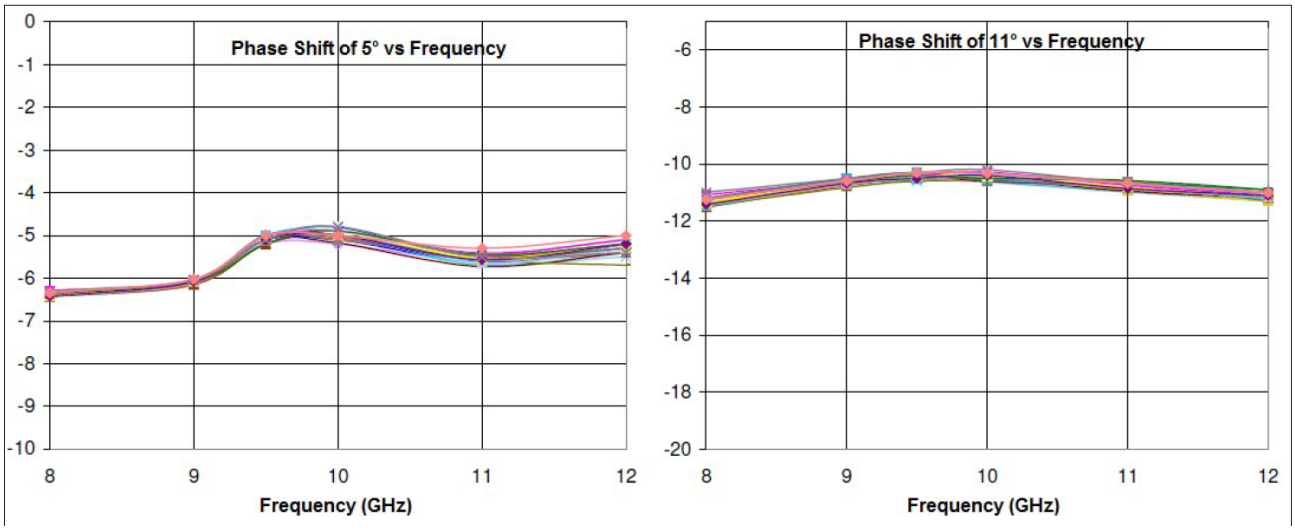
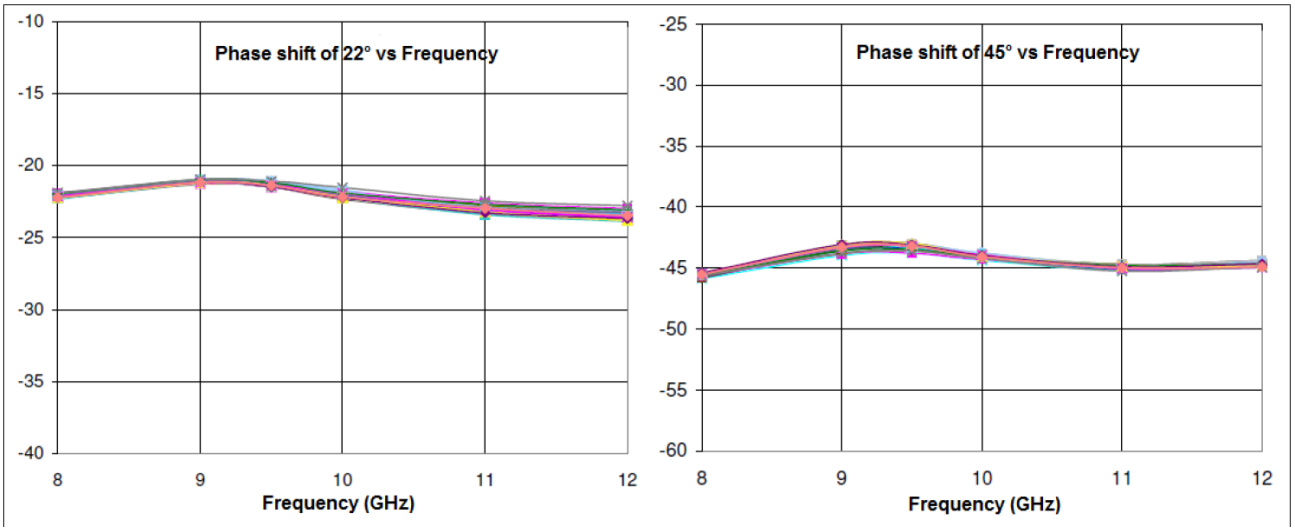
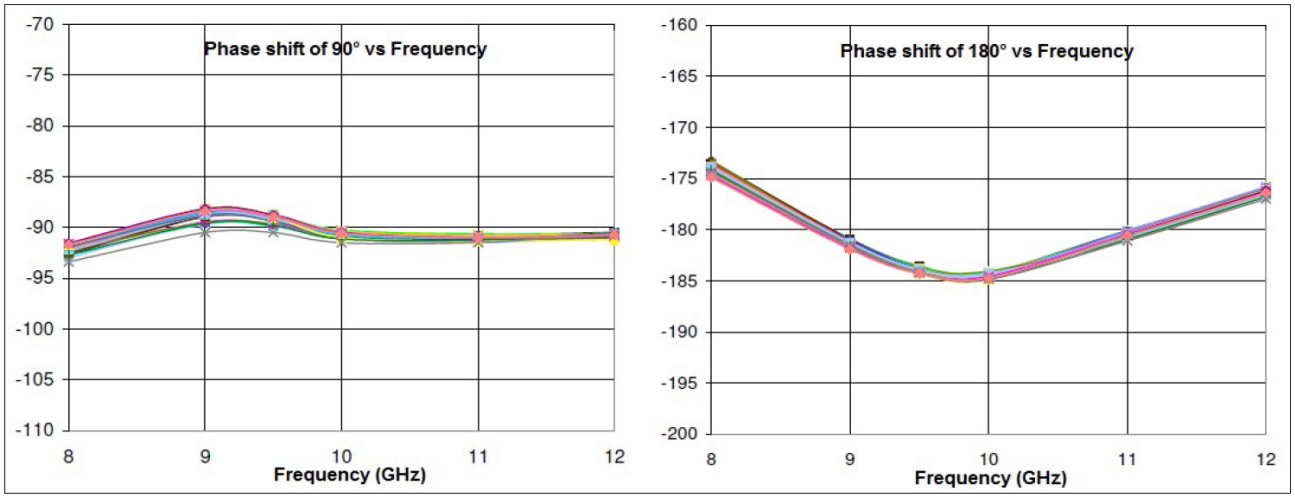
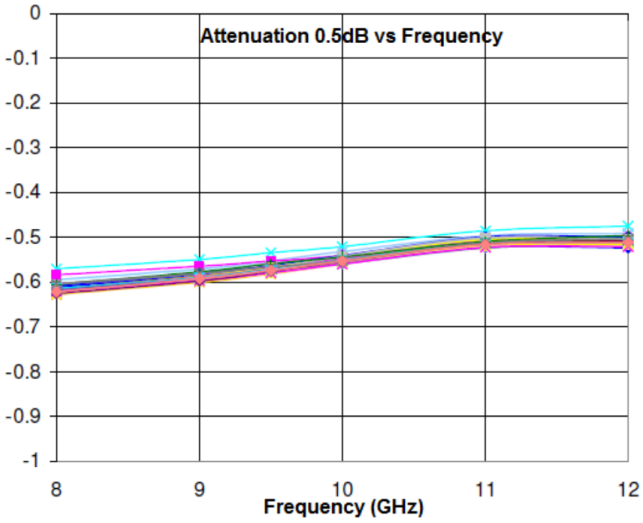
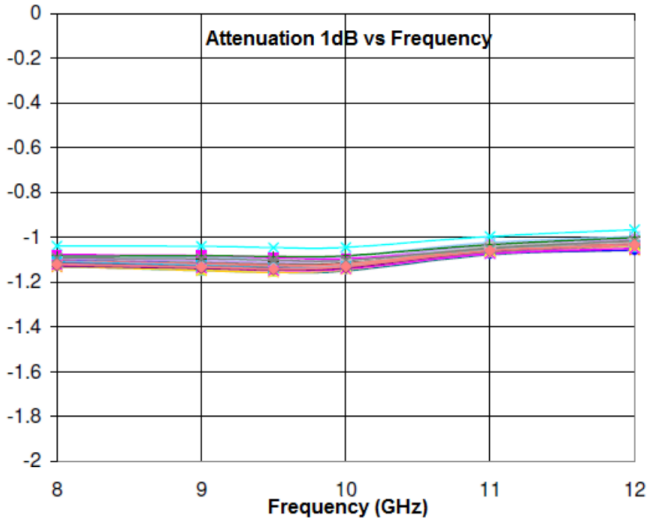


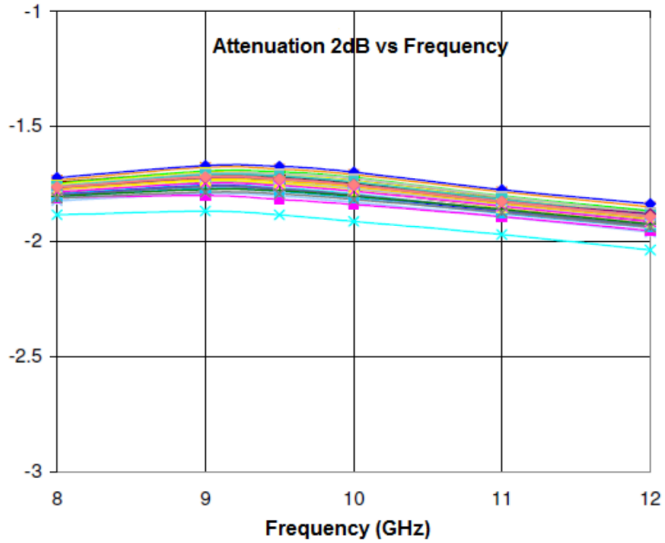


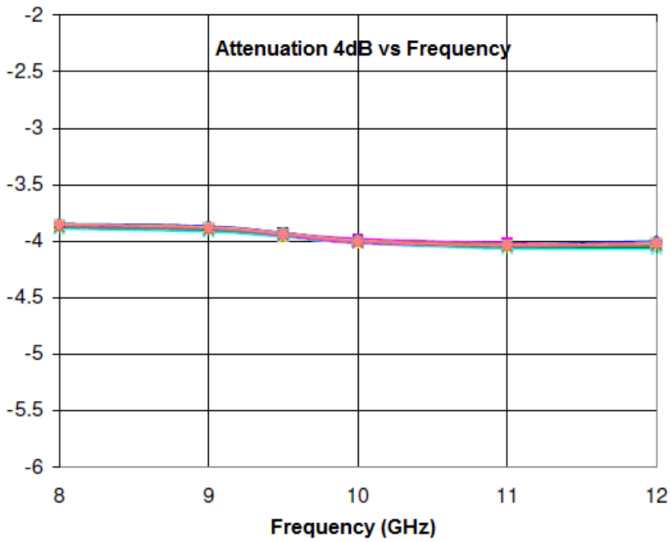


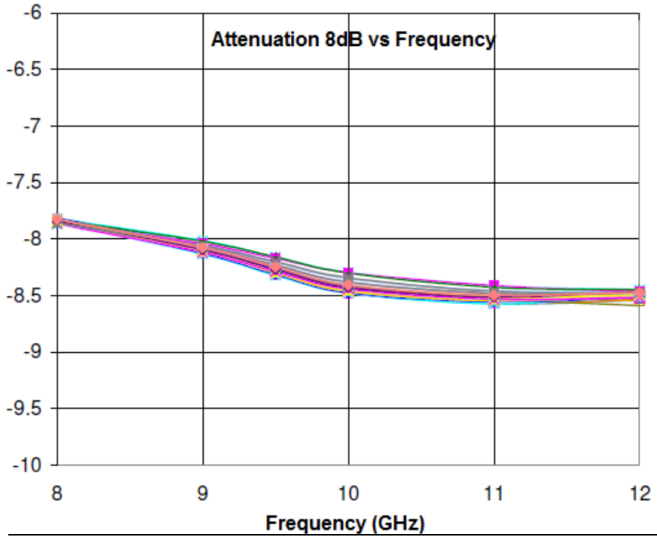
Typical Performance Curves: On board Measurements—Attenuator Response

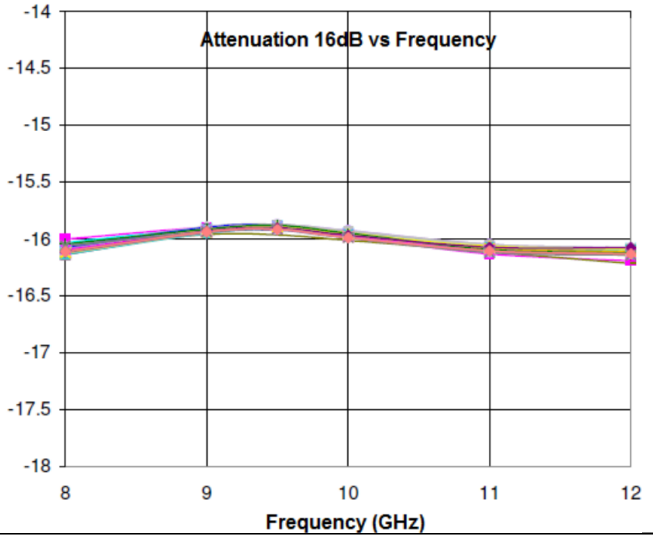




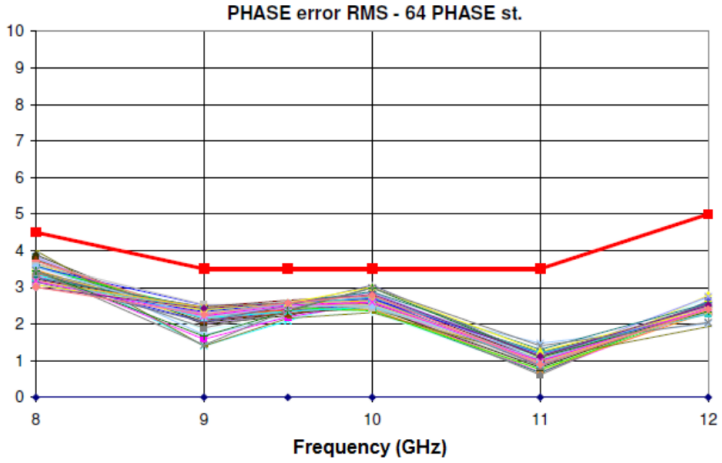


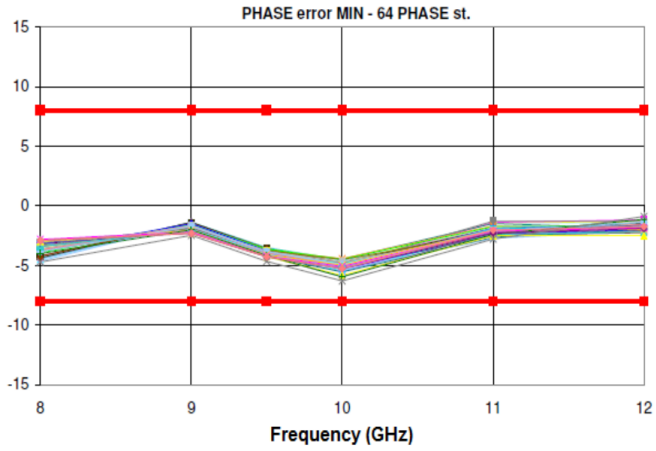


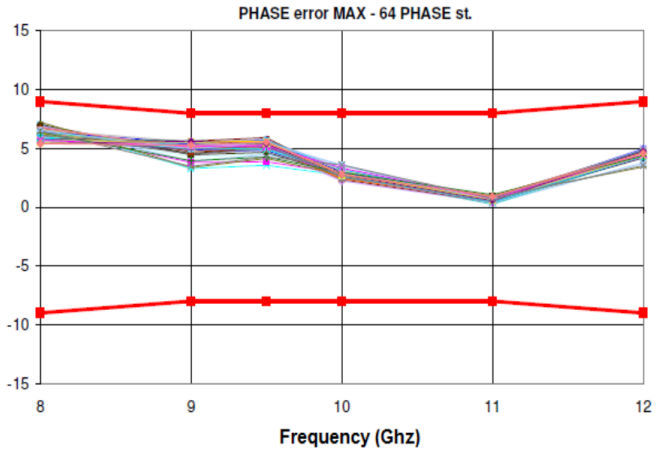


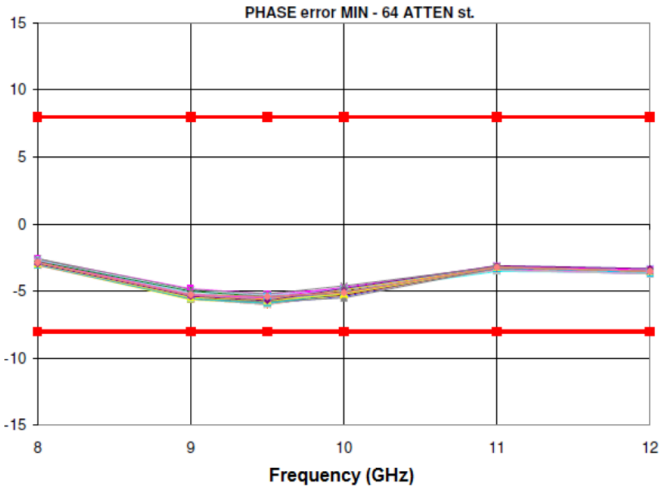


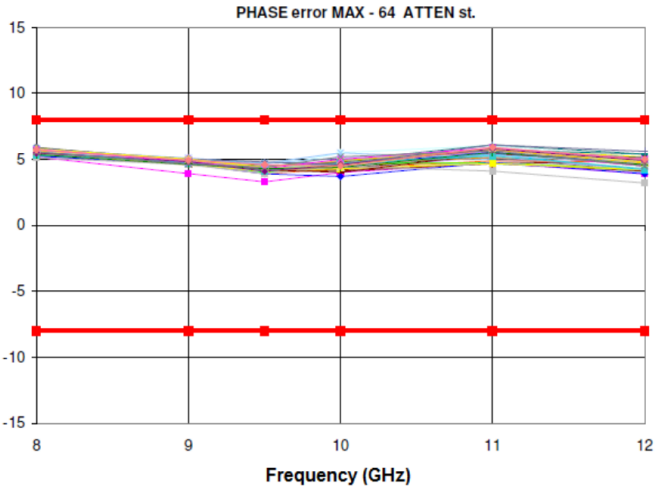
Typical Performance Curves: On board Measurements—Phase Shifter Errors



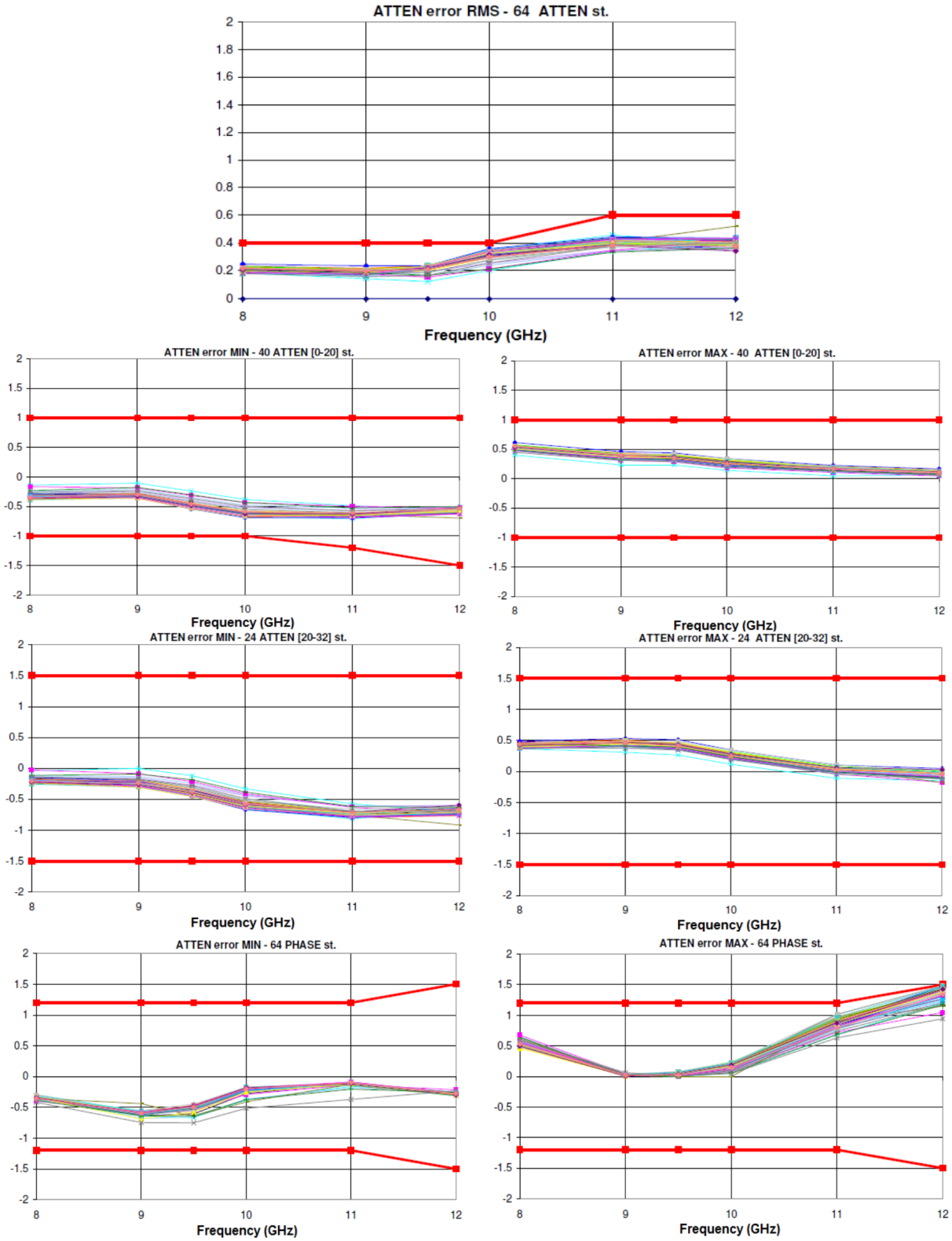




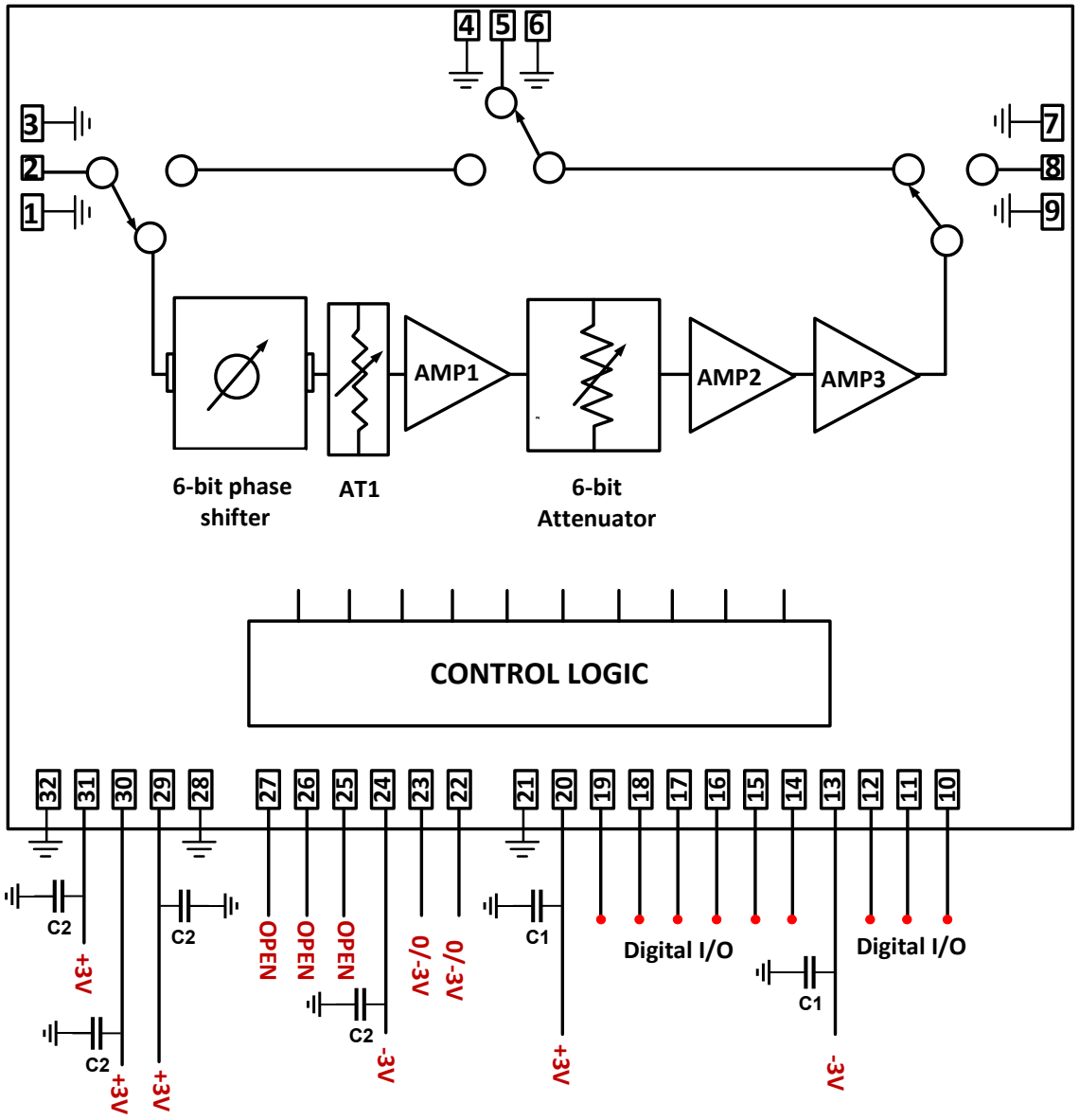




Typical Performance Curves: On board Measurements—Attenuation Errors



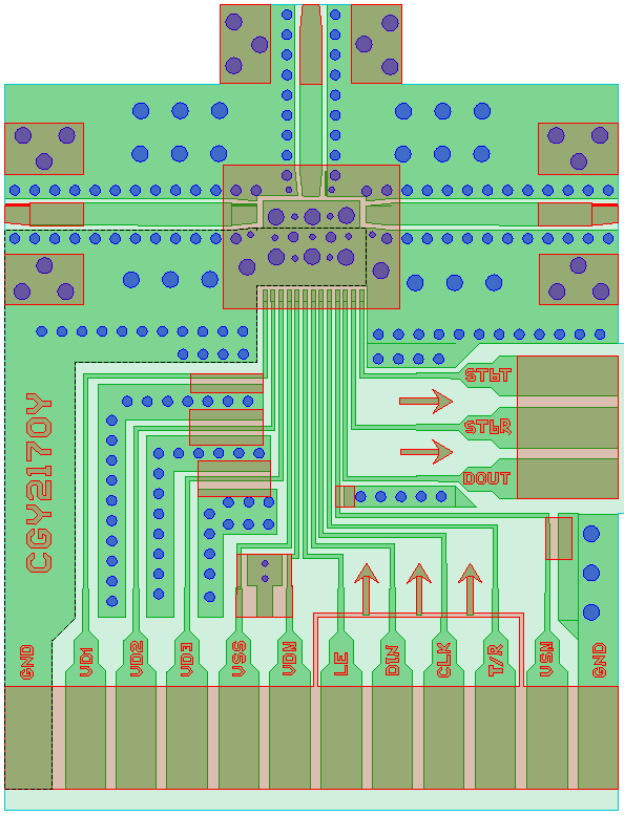
Functional Schematic



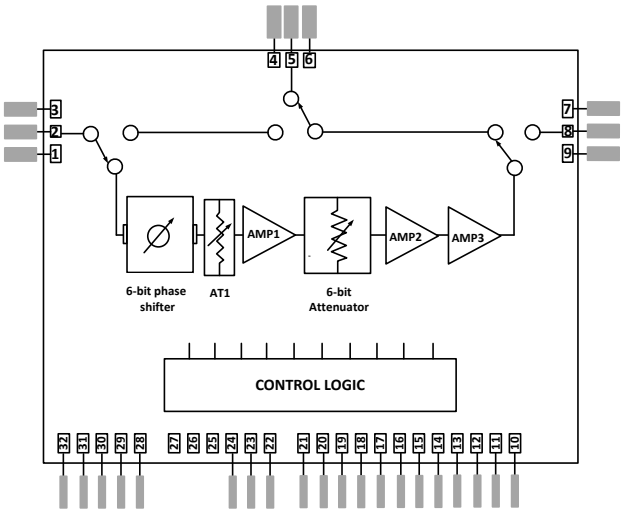
Parts List

Part	Value	Case Style	Manufacturer	Manufacturer's Part number
C1	100 nF	0402 INCH	Murata	GRM155R70J104KA01D
C2	10 nF	0402	Murata	GRT188R71E474KE13D

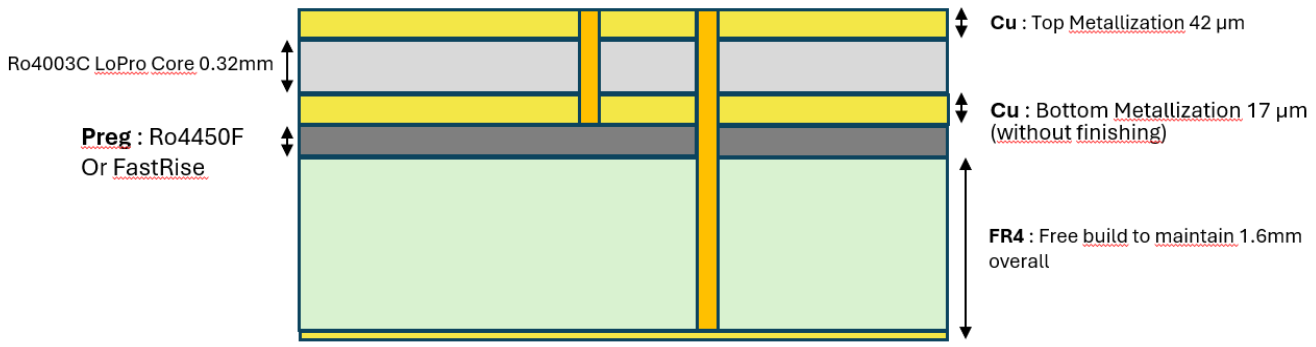
PCB Layout



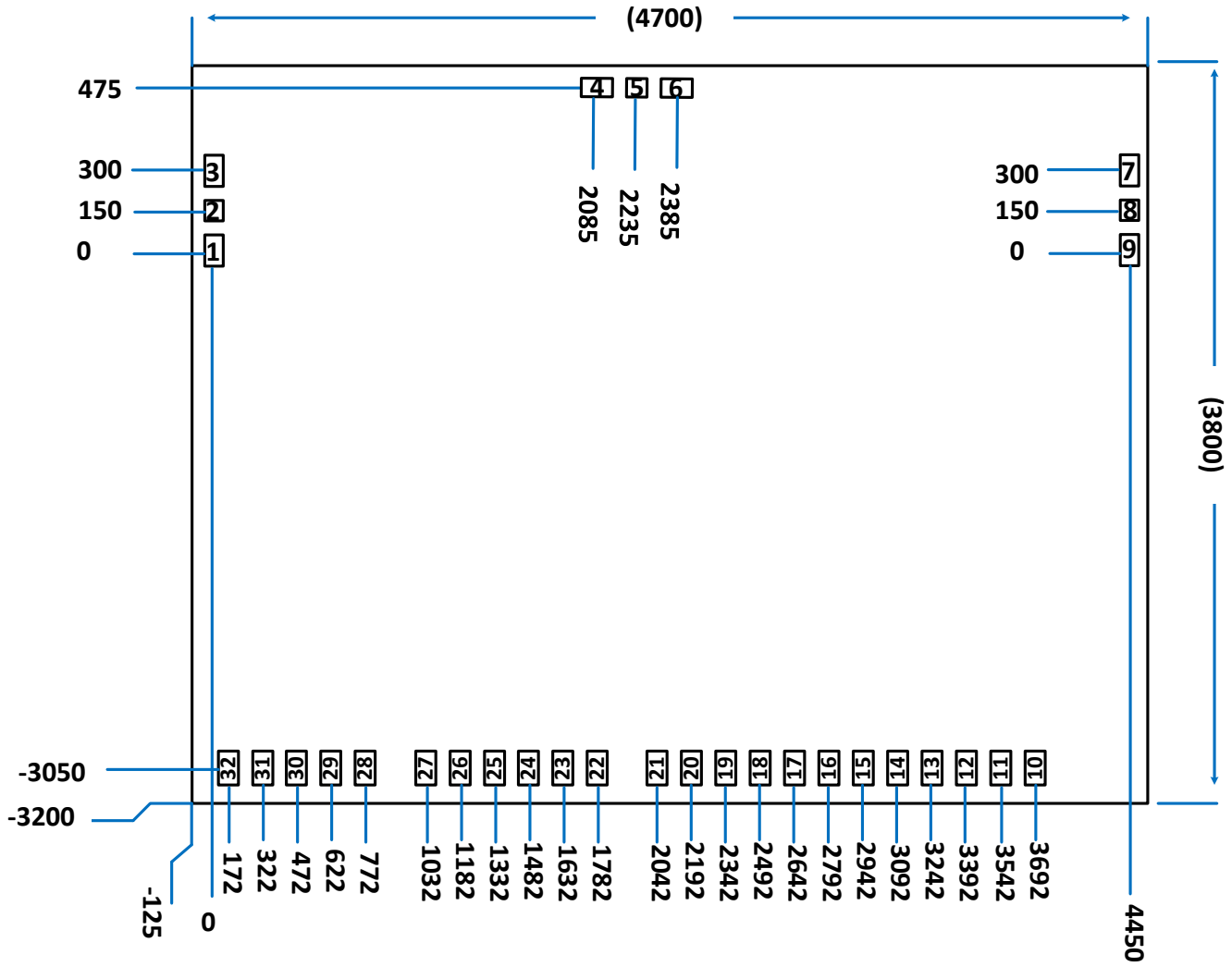
Functional Schematic



PCB Stack-up



Die Layout



Pads Dimensions

Pad #	X	Y
1,3,4,6,7,9	87	97
2,5,8	87	87
10-32	97	137

Revision History

Rev	Date	Change Description
V1	05/04/24	Initial Release
V2	01/28/25	Diagram block ,Diagram bonding, Functional schematic, Pads configuration, Die size