Features

- Suitable for 43 Gb/s Optical Fiber Links
- Wide Frequency Range: DC - 46 GHz
- Small Signal Gain: 16 dB
- 6.5 Vpp Output Swing in 50 Ω Load
- Power Consumption: 900 mW
- P1dB: 21 dBm @ 15 GHz
- Noise Figure: 2 dB @ 15 GHz
- Chip Size: 1270 x 1670 µm
- 100% RF Tested, Inspected Known Good Die
- Samples Available
- Space & MIL-STD Available
- RoHS* Compliant

Applications

- 43 Gb/s OC-768 Driver amplifier for LiNbO3 Modulator or Electro-Absorption Modulator (EAM)
- Instrumentation, EW Systems
- General Purpose Amplifier

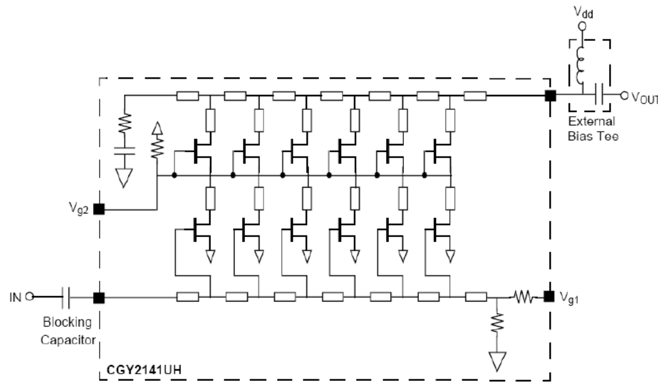
Description

The CGY2141UH/C1 is a distributed very wide band 43 Gb/s Electro-Absorption Modulator (EAM) / Lithium Niobate modulator driver. This device is a key component for ultra high speed optical communication systems (OC-768/STM-256).

This device can also be used as a flexible, multi-purpose, very wide band gain block from DC to 46 GHz. It features single-ended input and output and operates with a 5 V supply voltage via an external bias tee.

The MMIC is manufactured using a qualified 0.13 µm pHEMT GaAs D01PH technology. The D01PH process is one of the European Space Agency (ESA) European preferred part list (EPPL) technologies.

Block Diagram



Ordering Information

Part Number	Package
CGY2141UH/C1	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC Electrical Specifications: Freq. = DC - 46 GHz, V_{DD} = 5 V, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage Gate Supply Voltage 1 Gate Supply Voltage 2	— See note 1 —	V	+4.75 -4.50 0.00	+5.00 0.00 +1.50	+5.25 +4.50 +3.00
Supply Current Gate Supply Current 1 Gate Supply Current 2	—	mA	—	180 15.0 2.0	200 — 3.0

1. Vg1 determines the typical drain current. Vg1 should be raised slowly from -4.5 V until the drain DC current reaches 180 mA.

AC Electrical Specifications:
Freq. = DC - 46 GHz, V_{DD} = 5 V, V_{G2} = 1.5 V, I_{DD} = 180 mA, RL = 50 Ω, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Serial Data Rate	NRZ	Gb/s	43	—	—
Reference Gain	3 GHz[2]	dB	15	16	—
Gain Ripple[3]	100 MHz - 35 GHz 35 GHz - frequency cutoff	dB	-0.6 -3.0	—	+1.25
Frequency Cutoff	High (Gain 3 GHz - 3 dB) See note 4	GHz	44 —	46 —	— 50
Group Delay	3 - 33 GHz 33 - 40 GHz	ps	—	8 10	9 12
Output Swing Voltage Level	50 Ω Load, V_{IN_PP} = 1.5 V 50 Ω Load, V_{IN_PP} = 0.5 V	V	—	6.5 3.0	—
Rise/Fall Time	See note 5	ps	—	—	10
Input Return Loss	100 MHz - 22 GHz 22 - 35 GHz 35 - 45 GHz	dB	—	-10.0 -8.5 -5.5	-9.0 -7.0 -4.5
Output Return Loss	100 MHz - 40 GHz 40 - 45 GHz	dB	—	-17 -13	-11 -10
Jitter	See note 5	ps-rms	—	—	1
Noise Figure	5 - 35 GHz	dB	—	4	—
Output P1dB	1 - 30 GHz	dBm	—	19	—
Microwave Stability Factor	-10°C to +85°C, All passive source and load	-	1.2	—	—

2. Measurement is guaranteed by correlation down to the lower frequency cut-off. 3 GHz is specified as a reference for convenience of measurement.
3. Low frequency gain ripple assumes the use of drain decoupling close to the chip, as proposed on the figure 1 and 2.
4. The input and output are DC coupled. The low frequency cut-off is set by the choice of the input blocking capacitor or by the output bias tee used for drain current supply voltage.
5. Measurement limited by the input reference signal, cable losses, probes and connectors.

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Supply Voltage	-0.5 V to +8.0 V
Supply Current	240 mA
Gate Voltage 1	-7 to +7 V
Gate Voltage 2	-0.5 to +5.0 V
Junction Temperature	+150°C
Operating Temperature	-10°C to +85°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance	58°C/W

Handling Procedures

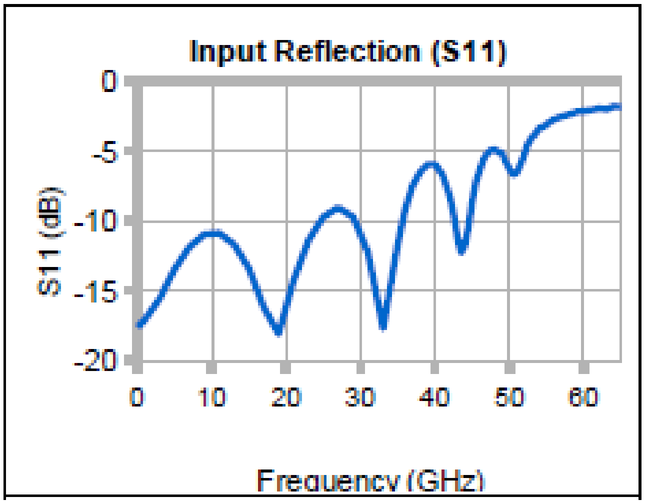
Please observe the following precautions to avoid damage:

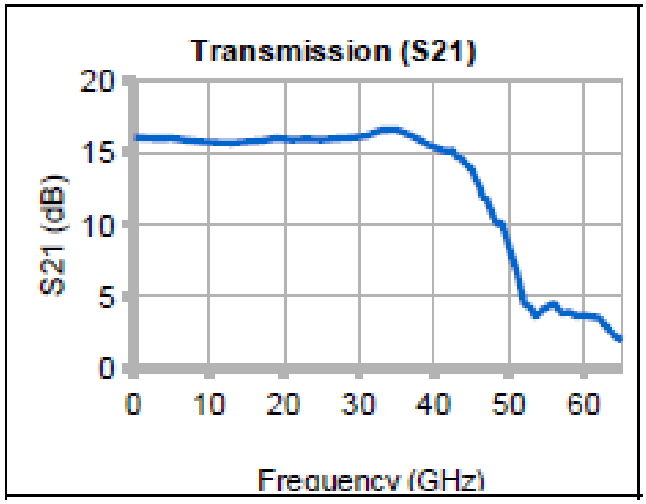
Static Sensitivity

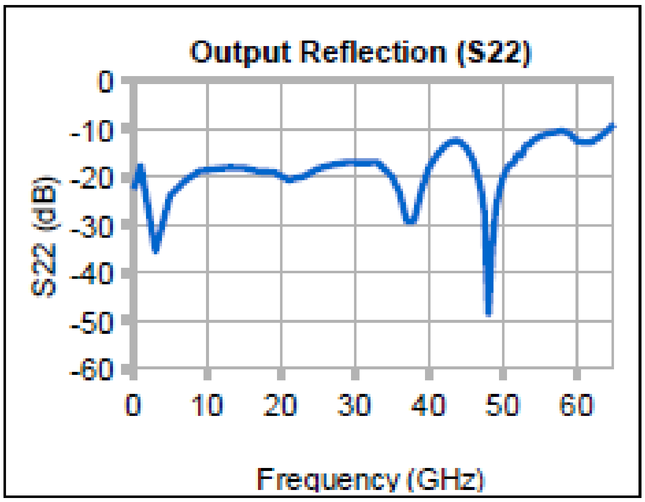
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

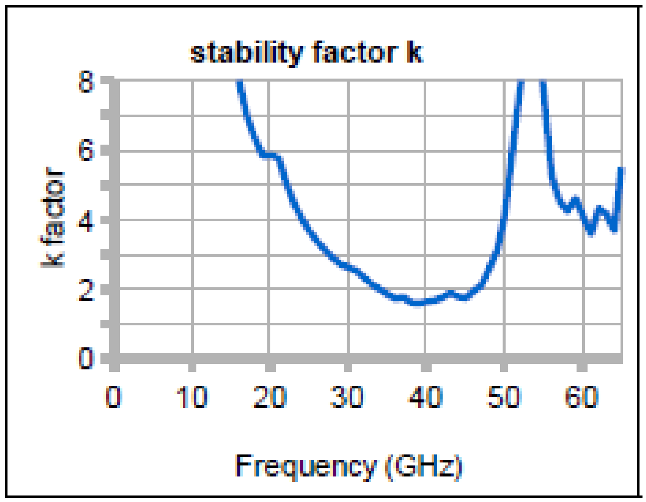
Typical Performance Curves: On Wafer

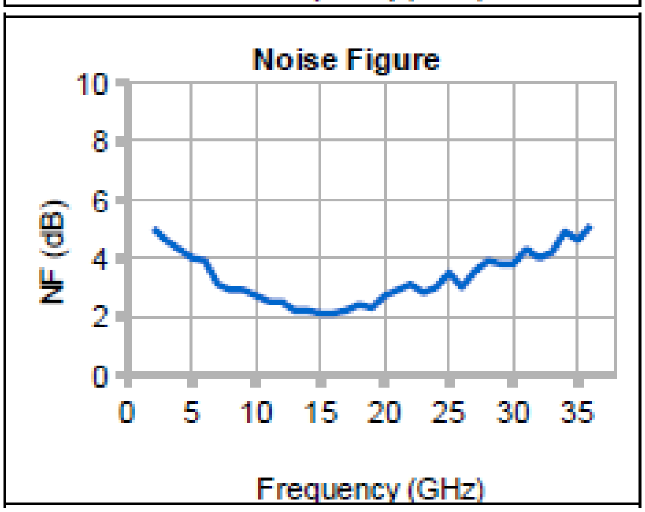
V_{DD} = 5 V, V_{G2} = 1.5 V, I_{DD} = 180 mA, V_{G1} = 0.0 V, T_A = +25°C

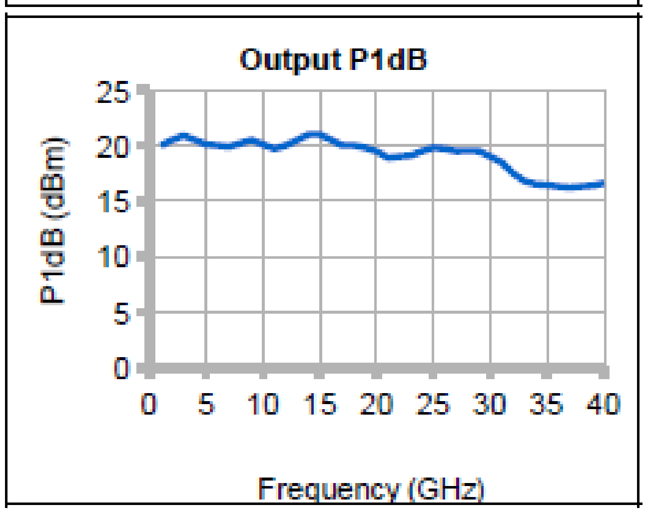












Application Information

Two module layouts are proposed in figure 1 and 2. In figure 1, RF input and output accesses are built in microstrip transmission line. While in figure 2, coplanar transmission line are used and will give similar performance. All path lengths and physical sizes of the components should be minimized.

All RF input and output bonding inductances should be minimized to give the best performance of the driver module. Two gold wires are recommended with maximum separation between the wires. Overall wire length should be kept less than 0.4 mm to keep lead inductance to less than 0.2 nH. Wedge-Wedge bonding is highly recommended for this purpose. Degradation of gain and match will be evident at higher RF input/output inductance. Ribbon bonding technique can also be used.

All others bonding inductances (pads Vdd1, Vdd2, Vg1, Vg2) should be kept as short as possible.

In figure 1 and figure 2, C1, C2 (47 pF) and C3, C4 (100 nF) capacitors are used to improve the power supply rejection, while C5 (100 nF) is used for low frequency gain extension. C6 is a link capacitor used to isolate the amplifier from external circuitry. C6 (100 nF) will give a low frequency cut-off down to a few kHz.

The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is extremely important to use an uninterrupted ground plane. AuSn or silver conductive epoxy material can be used for die attachment.

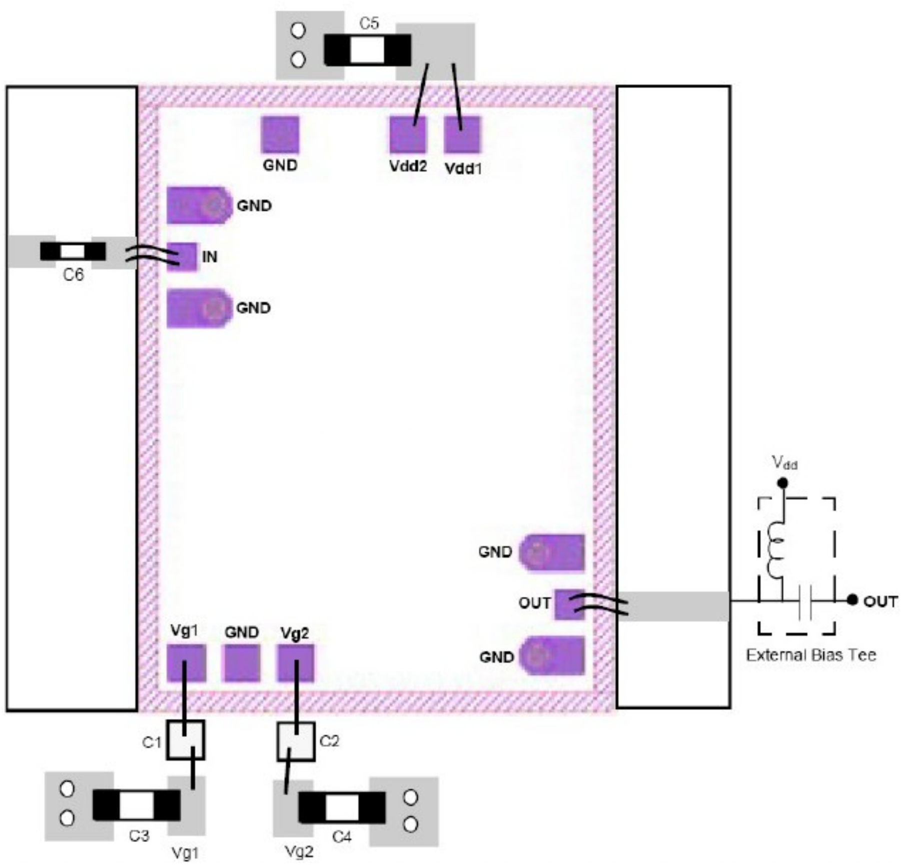


Figure 1: Module Layout: Microstrip Assembly

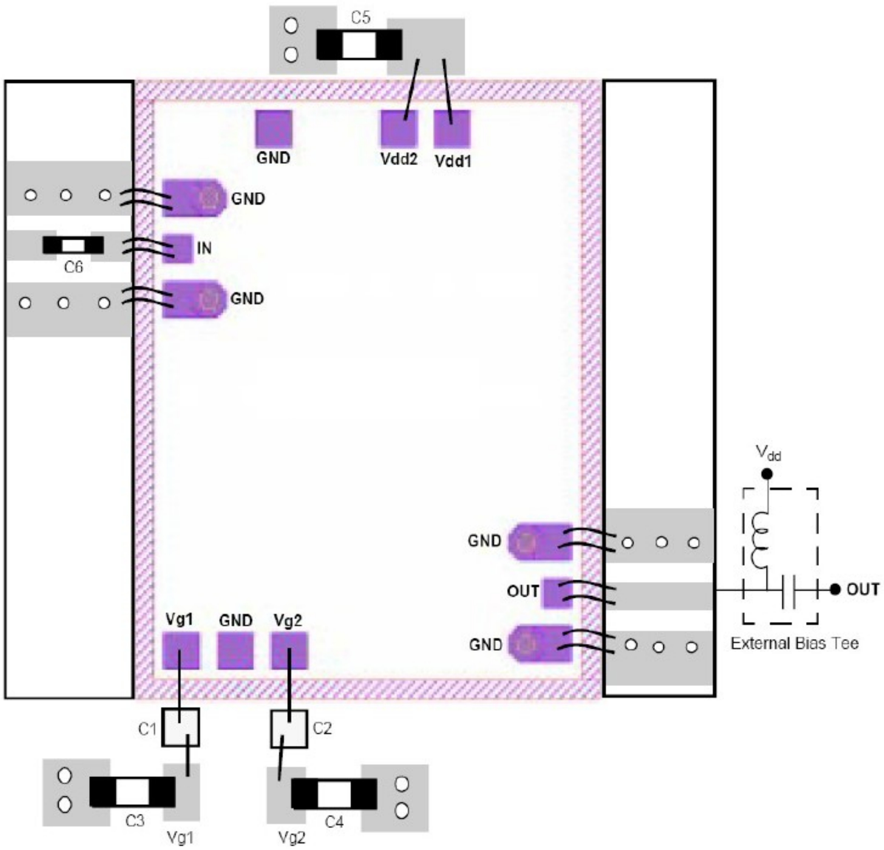


Figure 2: Module Layout: Coplanar Assembly

Operating & Handling Instructions

This device is a very high performance GaAs device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence

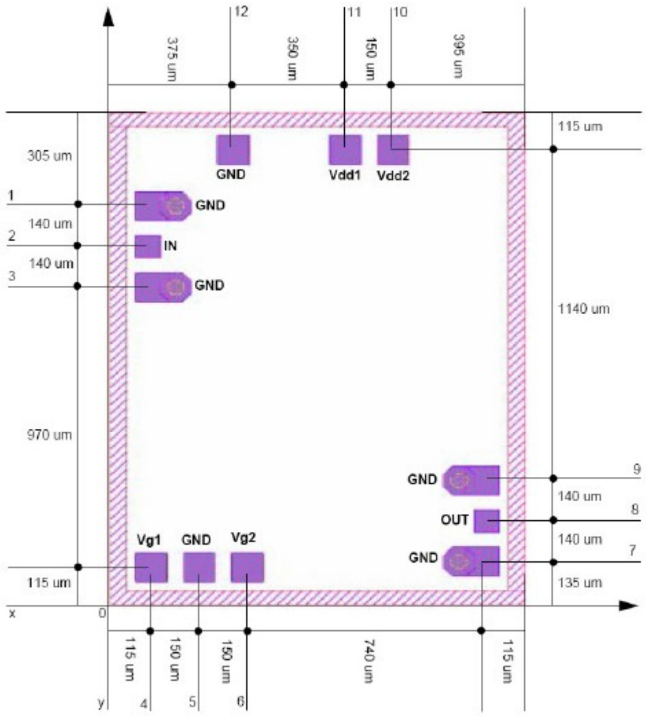
The following power supply sequence is recommended:

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting Vg1 to -4.5 V and Vg2 to 0.0 V.
c) Increase Vdd = 5.0 V while monitoring the drain current.
d) Increase Vg2 to 1.5 V
e) Increase Vg1 slowly from -4.5 V until the drain current reaches 180 mA.
f) Apply the RF input signal.

2- Mounting and ESD handling precautions

For high performance integrated circuits, care must be taken when mounting GaAs MMICs so as to correctly mount, bond and subsequently seal the packages and hence obtain the most reliable long-term operation.

Mechanical Information



Chip Size = 1670 x 1270 µm (Tolerance ± 15 µm)
DC Pads = 100 x 100 µm
RF Pads = 90 x 90 µm
Chip Thickness = 100 µm
Backside Metal = TiAu
Passivation = PECVD deposited Si3N4

Pad Position[8]

Pad Name	Pad#	Coordinate		Description
		X	Y	
GND	1	1365	115	Connected to ground with on-chip via hole
IN	2	1225	115	RF Input, used to connect VDD via bias Tee
GND	3	1085	115	Connected to ground with on-chip via hole
VG1	4	115	115	Gate supply voltage 1, must be decoupled to ground using external capacitors(s)
GND	5	115	265	Connected to ground with on-chip via hole
VG2	6	115	415	Gate supply voltage 2, must be decoupled to ground using external capacitors(s)
GND	7	135	1155	Connected to ground with on-chip via hole
OUT	8	275	1155	RF Output
GND	9	415	1155	Connected to ground with on-chip via hole
VDD2	10	1555	875	Drain low frequency extension pad 1, must be decoupled to ground using external capacitors(s)
VDD1	11	1555	735	Drain low frequency extension pad 2, must be decoupled to ground using external capacitors(s)
GND	12	1555	375	Connected to ground with on-chip via hole

8. X = 0, Y = 0 at bottom left corner.