

Power Amplifier, 33 dBm 18 - 23 GHz



CGY2135UH/C1

Rev. V1

Features

- P1dB: 31.2 dBm @ 20.5 GHz
- P_{SAT}: 32.3 dBm @ 20.5 GHz
- PAE: 20.2% @ 20.5 GHz @ P1dB
- Gain: 25.4 dB @ 20.5 GHz
- Power Supply: 4 V
- 50 Ω Input & Output Matched
- Input & Output Return Loss: 12 dB
- Chip Size: 3.65 x 3.14 x 0.1 mm
- Space and MIL-STD Available
- RoHS* Compliant

Applications

- Radar
- Telecommunication
- Instrumentation

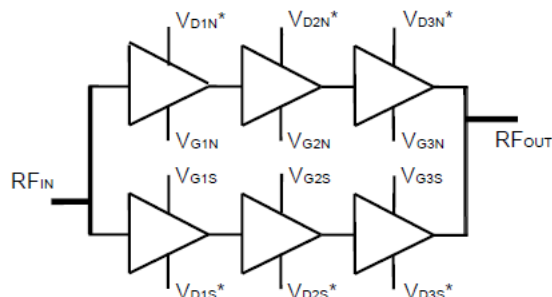
Description

The CGY2135UH/C1 is a high performance dual line-up 3 stage GaAs power amplifier MMIC designed to operate in the K band from 18 to 23 GHz.

The die is manufactured using the high performance 0.13 μm gate length pHEMT power technology D01PH. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram

V_{D1N}, V_{D2N}, V_{D3N} are available externally but are internally interconnected



V_{D1S}, V_{D2S}, V_{D3S} are available externally but are internally interconnected

Ordering Information

Part Number	Package
CGY2135UH/C1	DIE

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Measured On Wafer, $T_A = +25^\circ\text{C}$, $I_{DN} = I_{DS} = 600\text{ mA}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Drain Supply Voltage	—	V	—	4	—
Gate Supply Voltage	$I_{DN} + I_{DS} = 1200\text{ mA}$	V	—	-0.39	—
Total Supply Current	@ P_{SAT}	mA	—	1200	—
Gain	18.0 GHz	dB	—	23.9	—
	20.5 GHz			25.4	
	23.0 GHz			26.6	
Noise Figure	—	dB	—	TBD	—
P1dB	18.0 GHz	dBm	—	30.5	—
	20.5 GHz			31.2	
	23.0 GHz			32.3	
Saturated Power (P_{SAT})	18.0 GHz	dBm	—	31.8	—
	20.5 GHz			32.3	
	23.0 GHz			33.1	
Power Added Efficiency	—	%	—	20.2	—
Output IP3	—	dBm	—	TBD	—
IMD3	—	dBc	—	TBD	—
Reverse Isolation	RF_{OUT}/RF_{IN}	dB	—	-40	—
Input Return Loss	—	dB	—	12	—
Output Return Loss	—	dB	—	12	—
Leakage when HPA Off All Gates	—	dBm	—	TBD	—

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
Input Power	20 dBm
Voltage Gate Drain	-2.5 V to 0 V 0 to 5.5 V
Current Gate Drain	-1 to +1 mA 750 mA
Junction Temperature	+175°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +85°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance	8°C/W

Handling Procedures

Please observe the following precautions to avoid damage:

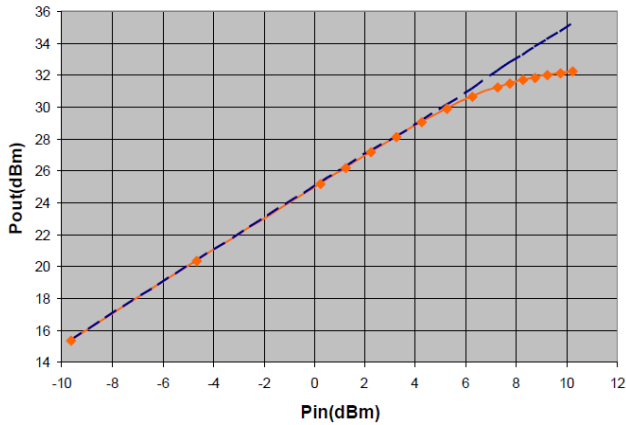
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

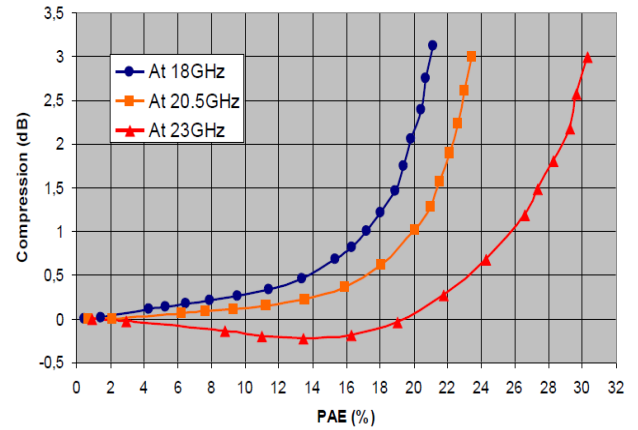
Typical Performance Curves: On Wafer Measurements

$V_{DN} = V_{DS} = 4\text{ V}$, $V_{GXN} = V_{GXS} = -0.4\text{ V}$ ($I_{DN} + I_{DS} = 1200\text{ mA}$), $T_A = +25^\circ\text{C}$

Output Power vs. Input Power

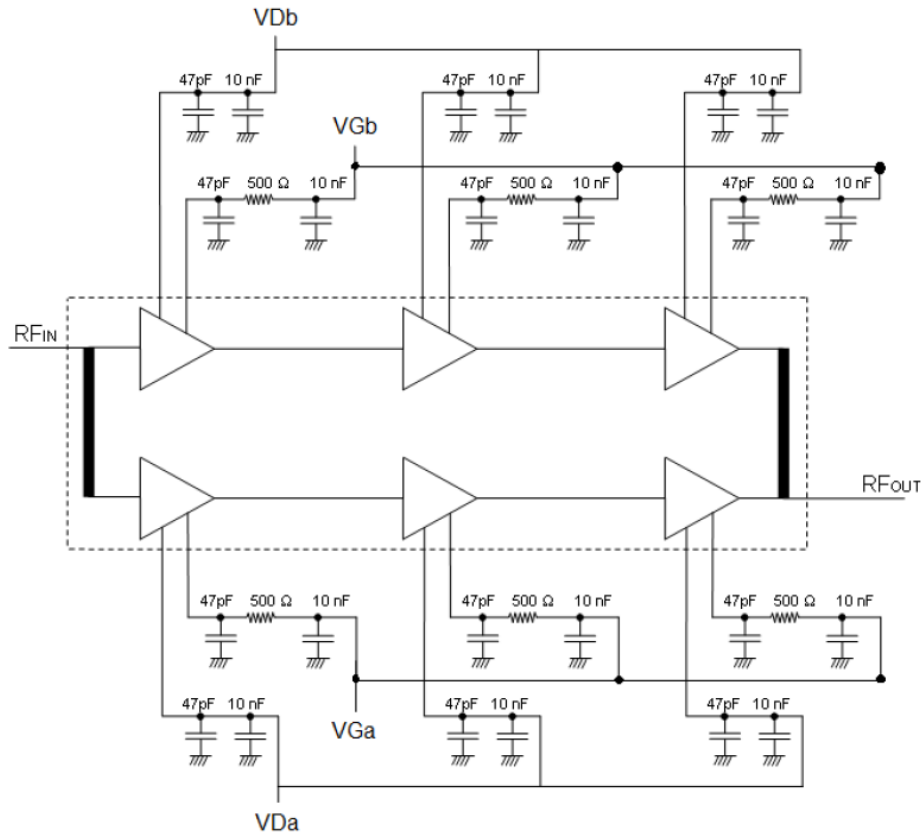


Compression vs. PAE



Application Schematic

To prevent instability of the customer design it is highly recommended to place a 47 pF RF decoupling chip capacitor at each DC terminal with the shortest possible bonding wires. Additionally, a 10 nF capacitor can be added on a drain connection. In the gate circuitry, a 500 Ω resistor have been added in series with each gate introducing some low pass filtering in case of fast power switching.

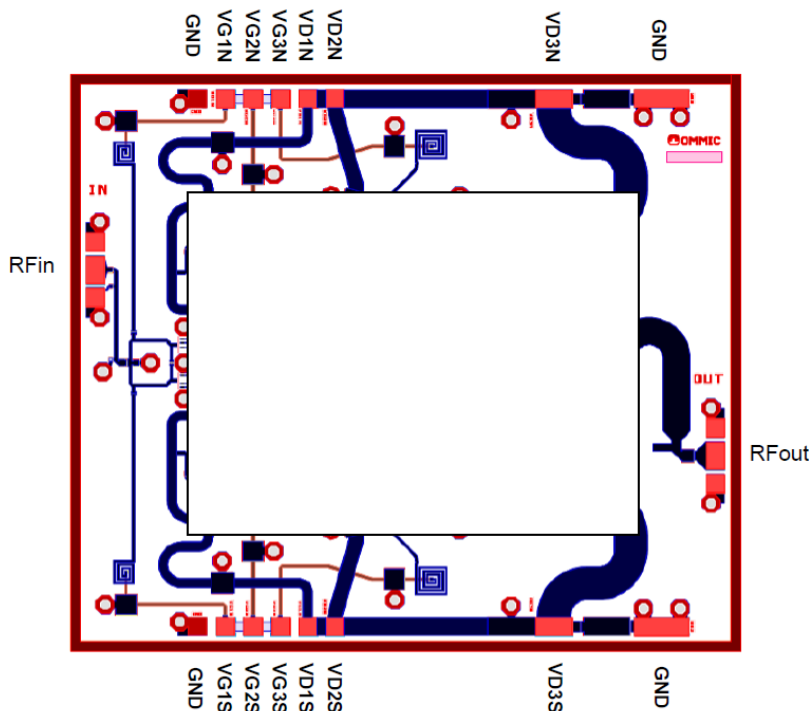


Component Name	Value	Type	Comment
All 47 pF capacitors	47 pF	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die with bonding as short as possible
All 500 Ω resistors	500 Ω	Chip Resistor	Chip resistor US MICROWAVES RG1421- 500-1% soldered close to the 47 pF chip capacitor with bonding as short as possible
All 10 nF capacitors	10 nF	Chip Capacitor	MURATA GMA085R71C103MD01T GM260 X7R 103M 16M100 PM520

Due to the highly symmetrical design of the component and the requirements of the power combiner, it is recommended to keep drain current I_{DN} equal to I_{DS} , for the same reason, it is recommended to keep drain voltage V_{DN} equal the V_{DS} .

In order to validate each stage of the amplifier with respect to the DC, it is recommended to set firstly all gate voltage V_{GXN} , X_S to -2 V, then to set the corresponding drain voltage V_{DN} , V_{DS} to +1 V and check that the corresponding drain current I_{DS} , I_{DS} stay at a very low level, after that verification, V_{DN} , V_{DS} can be set to 4 V. When V_{GXN} , X_S is changed from -2.5 V to roughly -0.4 V, the corresponding drain current increases slowly in a controlled manner to reach the typical targeted value.

Die Layout

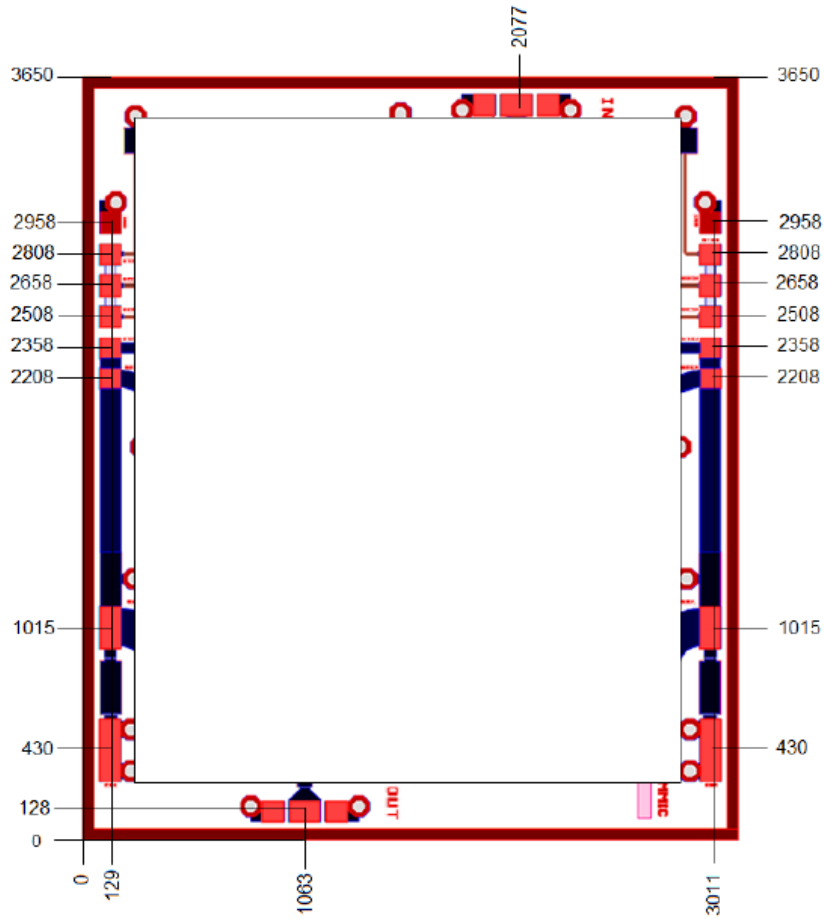


Pinout

Symbol	Pad	Description
RFOUT	Out	RF Output
RFIN	In	RF Input
VD3N	VD3B	Drain 3 Supply Voltage North
VD2N	VD2B	Drain 2 Supply Voltage North
VD1N	VD1B	Drain 1 Supply Voltage North
VG3N	VG3B	Gate 3 Supply Voltage North
VG2N	VG2B	Gate 2 Supply Voltage North
VG1N	VG1B	Gate 1 Supply Voltage North
VD3S	VD3A	Drain 3 Supply Voltage South
VD2S	VD2A	Drain 2 Supply Voltage South
VD1S	VD1A	Drain 1 Supply Voltage South
VG3S	VG3A	Gate 3 Supply Voltage South
VG2S	VG2A	Gate 2 Supply Voltage South
VG1S	VG1A	Gate 1 Supply Voltage South
GND	GND	Ground

3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Bonding Pad Coordinates



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