Low Noise Amplifier, Ka-Band
24 - 34 GHz

CGY2128UH/C2
Rev. V1

Features

- Noise Figure: 1.3 dB @ 29 GHz
- Small Signal Gain: 23 dB @ 29 GHz
- Low Power Consumption: <160 mW
- P1dB: 10 dBm @ 29 GHz
- 50 Ω Input & Output Matched
- Input Return Loss: >15 dB @ 29 GHz
- Output Return Loss: >15 dB @ 29 GHz
- Chip Size: 2.64 x 2.0 mm
- 100% RF Tested, Known Good Die
- Demonstration Boards Available
- Samples Available
- Flight Model
- RoHS* Compliant

Applications

- Ka Band
- Space Communication
- Instrumentation
- General Purpose

Description

The CGY2128UH/C2 is a high performance Ka band low noise amplifier. This device is a key component for high frequency systems.

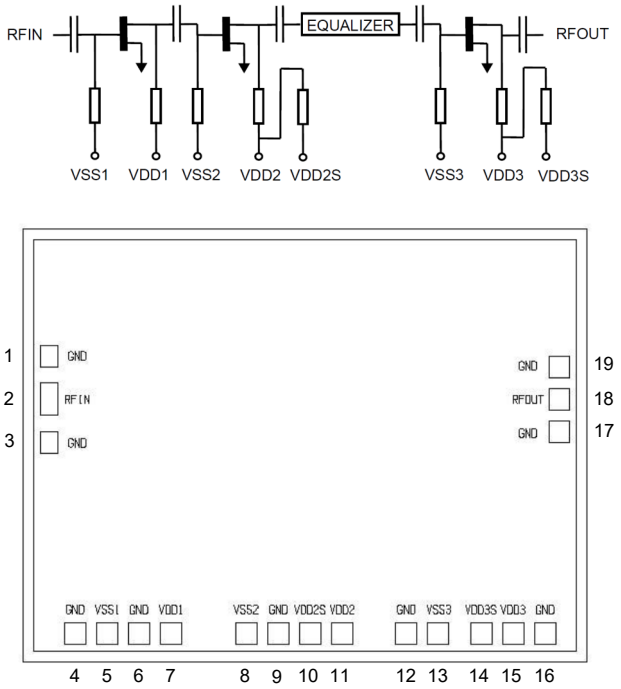
The CGY2128UH/C2 is a three stage low noise amplifier with a low power consumption (Vdd = 3.5 V, total drain current = 46 mA). It can be used as a replacement of CGY2128UH/C1 with identical RF performances, but easier management of space derating rules.

This device has two sets of drain voltage pads, one for commercial grade use, the second one imbedding automatic derating for space grade use.

The MMIC is manufactured using a proprietary 0.13 µm Metamorphic HEMT D01MH technology which is registered in the European Preferred Part List (EPPL) from European Space Agency (ESA).

Ordering Information

Part Number	Package
CGY2128UH/C2	Die



Pad Configuration[1]

Pad	Function
1,3,4,6,9,12,16,17,19	GND
2	RFIN
5	VSS1
7	VDD1
8	VSS2
10	VDD2
11	VDD2S
13	VSS3
14	VDD3S
15	VDD3
18	RFOUT

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Measured On Wafer, 50 Ω, no bonding (unless otherwise specified) Freq. = 24 - 34 GHz, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Drain Supply Voltage [2,3]	Commercial use (V_{DD2_S} & V_{DD3_S} left open) Space use (V_{DD2} & V_{DD3} left open)	dB	—	3.5 3.5	—
Drain Supply Current[2,3]	V_{SS1} gate voltage tuned V_{SS2} gate voltage tuned V_{SS3} gate voltage tuned	dB	—	8 13 25	—
Gate Supply Voltage[2,3]	tuning to each typical DC current	dB	-1.0	-0.7	0
Reference Gain[2,3]	with bonding wires	dB	19	23	—
Input Return Loss[2,3]	with bonding wires	dB	—	-16	-9
Output Return Loss[2,3]	with bonding wires	dB	—	-17	-9
Reverse Isolation	with bonding wires	dB	—	-48	—
Noise Figure[4]	@ 29 GHz, no bond wires	dB	—	1.6	2.0
P1dB	@ 29 GHz, no bond wires Commercial[2] Space[3]	dBm	9.0 7.0	10.5 8.5	—
Output IP3	2 SCL, 100 MHz Spacing 27.95 GHz[2] 28.05 GHz[3]	dBm	—	19.5 17.5	—

2. Commercial $V_{DD1} = V_{DD2} = V_{DD3}$ = 3.5 V, (V_{DD2_S}, V_{DD3_S} left open), I_{D1} = 8 mA, I_{D2} = 13 mA, I_{D3} = 25 mA.
3. Space $V_{DD1} = V_{DD2\_S} = V_{DD3\_S}$ = 3.5 V, (V_{DD2}, V_{DD3} left open), I_{D1} = 8 mA, I_{D2} = 13mA, I_{D3} = 25 mA.
4. Noise is improved by approximately 0.4 dB when mounted on carrier with bonding wires.

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
RF CW Input Power	10 dBm
Gate Voltage	-2 to +0.7 V
Drain Voltage	0 to +5 V
Drain Current V_{DD1} V_{DD2} V_{DD3}	 16 mA 26 mA 50 mA
Gate Current	10 mA
Junction Temperature Space Commercial	 +110°C +150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance	58°C/W

Handling Procedures

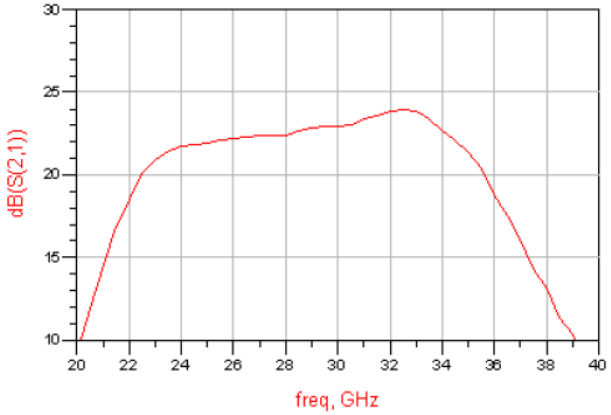
Please observe the following precautions to avoid damage:

Static Sensitivity

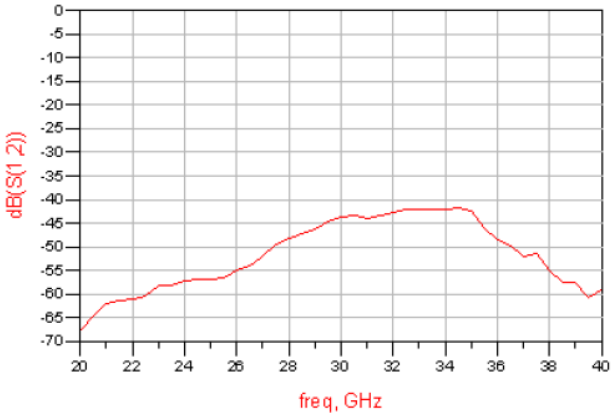
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves[7,8]: On wafer test, bonding wires added by calculation 20 fF/0.08 nH, 0.15 nH/20 fF.

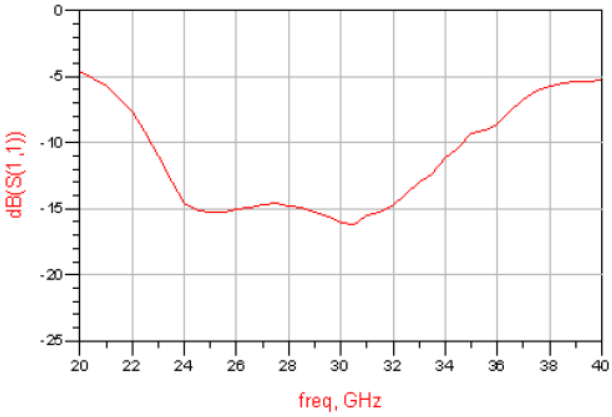
Gain vs. Frequency



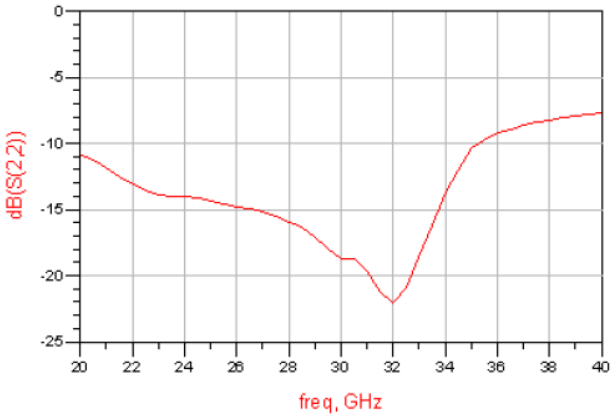
Reverse Isolation vs. Frequency



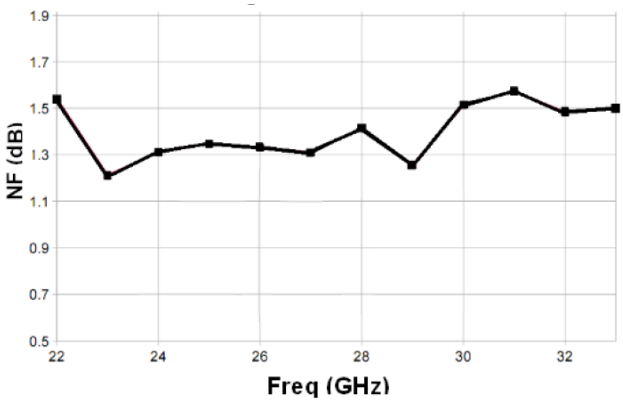
Input Return Loss vs. Frequency



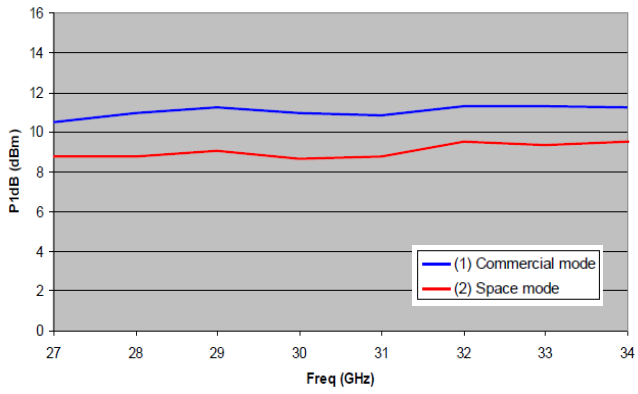
Output Return Loss vs. Frequency



Noise Figure vs. Frequency



P1dB vs. Frequency



7. Commercial and Space biasing modes have identical RF performances for S-parameters, Gain and Noise figure.
8. P1dB and OIP3 of Space mode are 2 dB lower than commercial mode.

Application Schematic

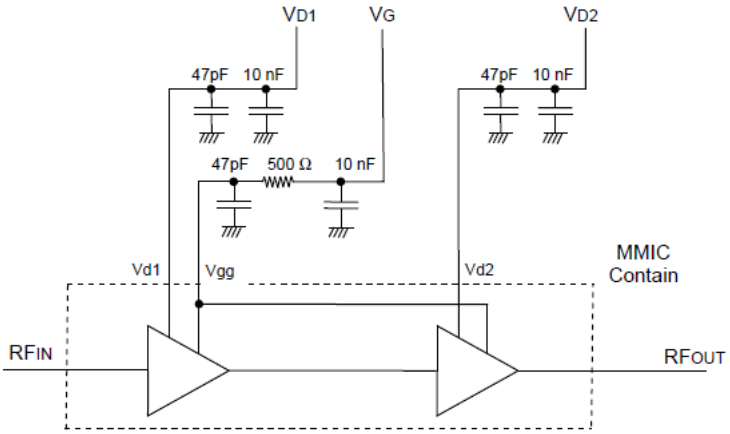
To prevent instability of the customer design it is highly recommended to place small chip capacitors as near as possible to the GY2125AUH/C1 die and to connect them with bondings as short as possible.

An additional 10 µF can also added on drain supplies in order to improve stability at low frequencies.

Additionally, a 10 nF capacitor can be added on a drain connection. In the gate circuitry, a 500 Ω resistor may be added in series to improve gate isolation and prevent unwanted oscillations. The resistors are introducing some low pass filtering in case of fast power switching using gate control architecture.

Depending on 50 Ω connected lines and associated tapers, many connections schemes can be studied/ used regarding RFin and RFout connections.

RFin and RFout bond wires can be two 25 µm wires bonding or one 50 µm ribbon.



Bonding Pad Coordinates

OPERATING AND HANDLING INSTRUCTIONS:

The CGY2128UH/C2 is very high performance MHEMT device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence
The following power supply sequences are recommended:

Power up :
1. Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
2. Set VDD1 ,VDD2 (or VDD2S) and VDD3 (or VDD3S) to 0 V
3. Pinch off the device by setting Vss1, Vss2, Vss3 to -1 V (gate current must be near 0 mA).
4. Increase VDD1 ,VDD2 (or VDD2S) and VDD3 (or VDD3S) to 3.5 V (drain current must stay near 0 mA)
5. Increase the gate voltages VSS1, VSS2 and VSS3 slowly from -1 V until the three drains current stages reaches respectively 8 mA, 13 mA and 25 mA.
6. Apply the RF input signal.

Power down :
1. Remove RF input signal
2. Pinch off the device by setting Vss1, Vss2, Vss3 to -1 V (gate and drain current must be near 0 mA).
3. Set VDD1 ,VDD2 (or VDD2S) and VDD3 (or VDD3S) to 0 V
4. Set VSS1, VSS2 and VSS3 to 0 V

Soldering

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn.

Toxic fumes will be generated at temperatures higher than 400°C.

Bonding Pad Coordinates

PAD LAYOUT

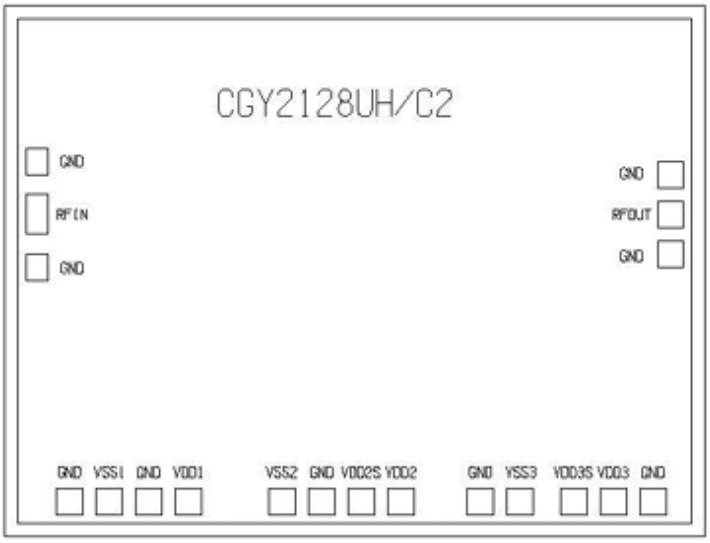


Figure 3: CGY2128UH/C2 Pad layout

PAD COORDINATES

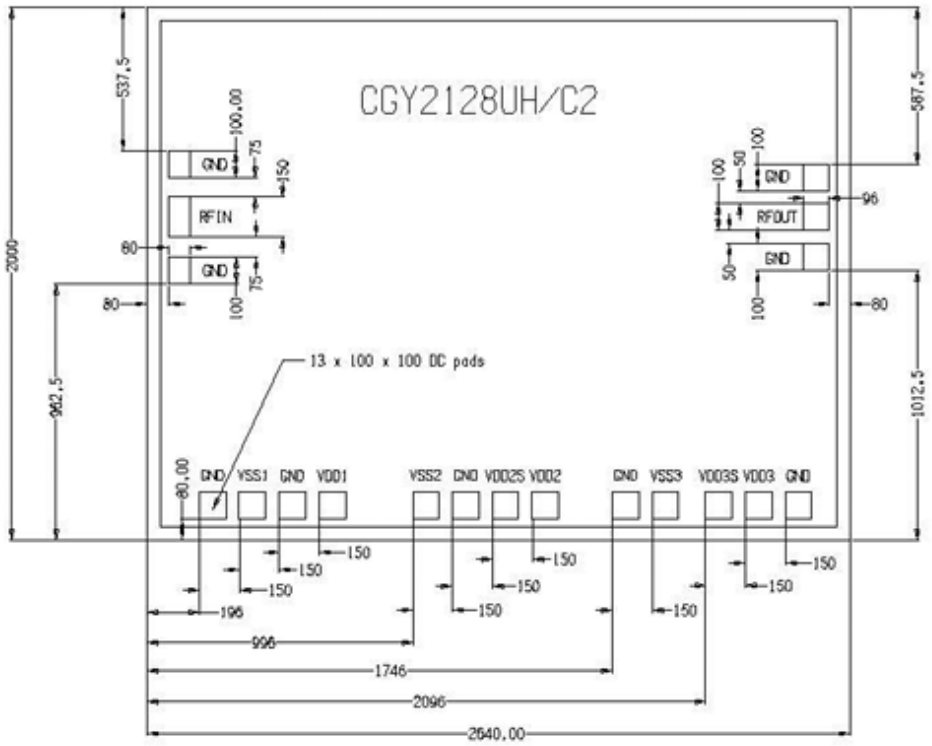


Figure 4: CGY2128UH/C2 pad coordinates

PAD POSITION

SYMBOL	PAD	COORDINATES		PAD SIZE	DESCRIPTION
		X	Y		
GND	1	122	1013	80 x 100	Connected to backside using via hole
RF IN	2	121	1213	80 x 150	RF input (RF probe pitch 200um)
GND	3	122	1413	80 x 100	Connected to backside using via hole
GND	4	245	130	100 x 100	Connected to backside using via hole
V_{SS1}	5	395	130	100 x 100	Gate supply 1
GND	6	545	130	100 x 100	Connected to backside using via hole
V_{DD1}	7	695	130	100 x 100	Drain supply 1
V_{SS2}	8	1046	130	100 x 100	Gate supply 2
GND	9	1195	130	100 x 100	Connected to backside using via hole
V_{DD2}	10	1345	130	100 x 100	Commercial Drain supply 2
V_{DD2S}	11	1495	130	100 x 100	Space application Drain supply 2
GND	12	1795	130	100 x 100	Connected to backside using via hole
V_{SS3}	13	1945	130	100 x 100	Gate supply 3
V_{DD3S}	14	2145	130	100 x 100	Space application Drain supply 3
V_{DD3}	15	2295	130	100 x 100	Commercial Drain supply 3
GND	16	2445	130	100 x 100	Connected to backside using via hole
GND	17	2512	1063	100 x 100	Connected to backside using via hole
RF OUT	18	2512	1213	100 x 100	RF Output (RF probe pitch 150um)
GND	19	2512	1363	100 x 100	Connected to backside using via hole

MECHANICAL INFORMATION

PARAMETER		DESCRIPTION
Size		2640 x 2000 mm
Thickness		100 µm
Backside material		TiAu
Passivation		PECVD deposition Si_3N_4
Boundings pad dimensions	GND	100 x 100 µm
	RF OUT, V_{DD3}, V_{DD3S}, V_{DD2}, V_{DD2S}, V_{DD1}, V_{SS3}, V_{SS2}, V_{SS1}	100 x 100 µm
	RF IN	80 x 150 µm

Note :
The die size and all pad positions refer to the mask layout, with (X=0, Y=0) at the bottom left corner of the layout. For each pad, the (X,Y) coordinates refer to the center of the pad.
Wafers are diced by sawing, with a saw line width of 35 µm (± 5 µm). A misalignment of the saw line with the middle of the dicing street (± 20 µm on all sides) may also result in a variation of ± 20 µm of the actual positions of the pads on the diced chip and an additional tolerance of ± 40 µm on the die size.

GENERAL APPLICATION INFORMATION

Typical application Information:

A reference device environment layout is proposed below. In this figure 1, RF input and output microstrip transmission lines are used, but coplanar transmission lines with similar performance may also be used. All path lengths and physical sizes of the components should be minimized. RF input bonding inductances should be minimized to give the best performance. Overall wire length should be kept as small as possible to reduce parasitic inductance. Higher RF input / output inductance may result in a degradation of gain and match. Ribbon bonding technique can also be used. The target inductance at the input is 0.08 nH, corresponding to 2 wires of 180 µm length. RF output bonding inductances should be minimized to give the best performance. Overall wire length should be kept as small as possible to reduce parasitic inductance. Higher RF input / output inductance may result in a degradation of gain and match. Ribbon bonding technique can also be used. The target inductance at the output is 0.15 nH, corresponding to 1 wire of 180 µu length.

All others bonding inductances (pads VDD1, VDD2, VDD2_S, VDD3, VDD3_S and Vss1, Vss2, Vss3) should be kept as short as possible. Decoupling 47 pF chip capacitors (close to the chip) and 10 nF chip capacitors are used to improve the power supply rejection. High value, additional decoupling capacitor in SMD format can be added. The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is extremely important to use an uninterrupted ground plane. AuSn eutectic soldering or silver conductive epoxy material can be used for die attachment.

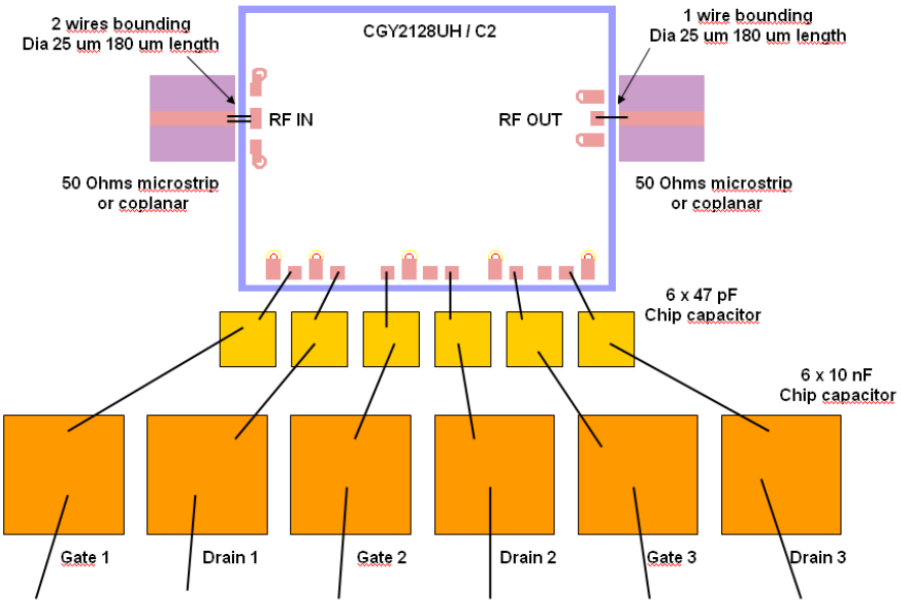


Figure 1: CGY2128UH/C2 commercial application mounting scheme