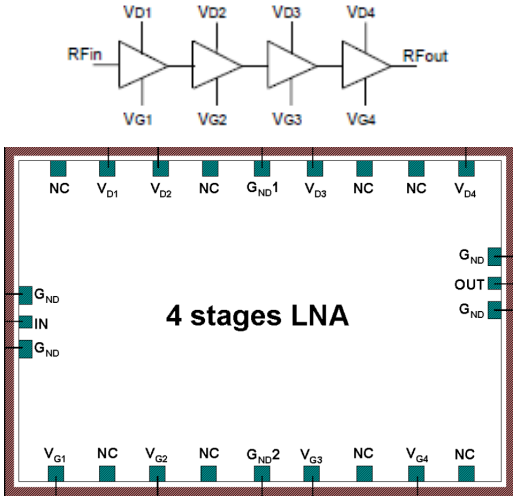
Ultra Low Noise Amplifier
25 - 43 GHz

CGY2122XUH/C2
Rev. V1

Features

- Noise Figure: 1.5 dB
- Gain: 32 dB
- Input Return Loss: >8 dB
- Output Return Loss: >8 dB
- Power Supply: 30 mA @ 1.1 V
- Die Size:3 x 2 mm
- 100% RF Tested, Inspected Known Good Die
- Demonstration Boards Available
- RoHS* Compliant



Applications

- Radar
- Telecommunication
- Instrumentation
- SATCOM

Description

The CGY2122XUH/C2 is a high performance GaAs Low Noise Amplifier MMIC designed to operate in the K band.

This device has an exceptionally low noise figure of 1.2 dB with a very flat 19 dB of gain (+/-0.4 dB). The on chip matching provides 12 dB of input return loss and 11 dB of output return loss. Thanks to the DC regulation the gain and noise are very stable with regards to temperature change. It can be used in Radar, Telecommunication and Instrumentation applications.

The die is manufactured using an advanced 70 nm gate length high Indium content MHEMT Technology. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

Pad Configuration

Pad	Function
RF_{OUT}	RF Output
RF_{IN}	RF Input
VD1	First Stage Drain
VD2	Second Stage Drain
VD3	Third Stage Drain
VD4	Forth Stage Drain
VG1	First Stage Gate
VG2	Second Stage Gate
VG3	Third Stage Gate
VG4	Forth Stage Gate
GND1	Ground
GND2	Ground
N/C	No Connection
GND[1]	Backside Pad

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package
CGY2122XUH/C2	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications[2]: Freq. = 25 - 43 GHz, T_A = +25°C, V_D = +1.1 V, I_D = 7.5 mA

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	—	32	—
Minimum Noise Figure	32 GHz	dB	1.2	—	—
Noise Figure	—	dB	—	1.5	—
Supply Voltage	—	dB	—	1.1	—
Supply Current	$V_{D1,2,3,4}$ = 1.1 V	dB	—	30	—
Reverse Isolation	RF_{OUT} / RF_{IN}	dB	—	-50	—
P1dB	—	dBm	—	1.2	—
Output IP3	—	dBm	—	10	—
Input Return Loss	50 Ω	dB	—	—	-8
Output Return Loss	50 Ω	dB	—	—	-8

2. Performance on Reference Board @ 29 GHz.
3. Measured reference plane are the input and output planes of the MMIC.

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
RF Input Power	1 dBm
Gate Voltage	-2.5 to 0 V
Drain Voltage	0 to +1.2 V
Drain Current	50 mA
Gate Current	-1 to +1 mA
Junction Temperature	+175°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +85°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance	TBD°C/W

Handling Procedures

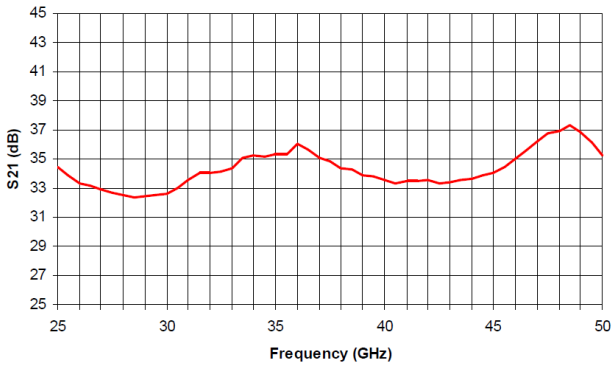
Please observe the following precautions to avoid damage:

Static Sensitivity

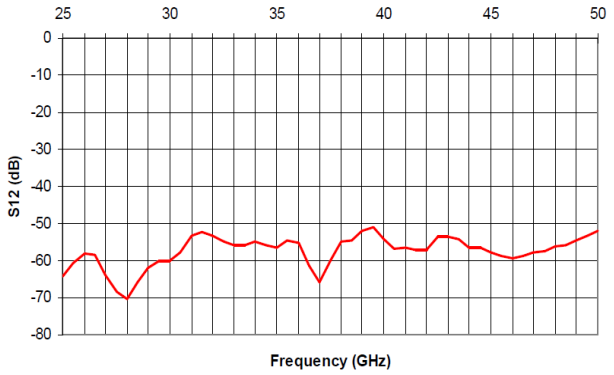
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: V_D = 1.1 V, I_D = 7.5 mA, T_A = +25°C

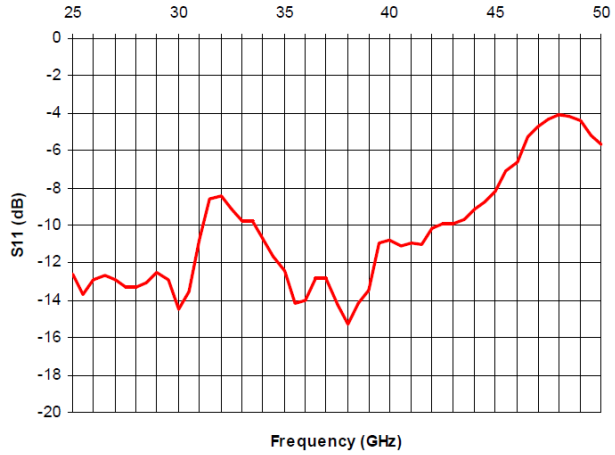
Gain vs. Frequency



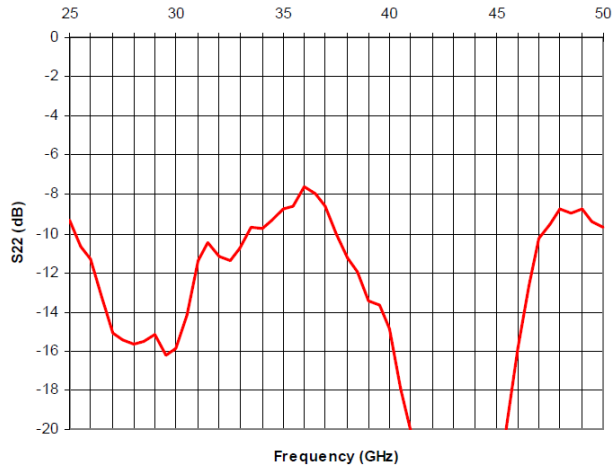
Reverse Isolation vs. Frequency



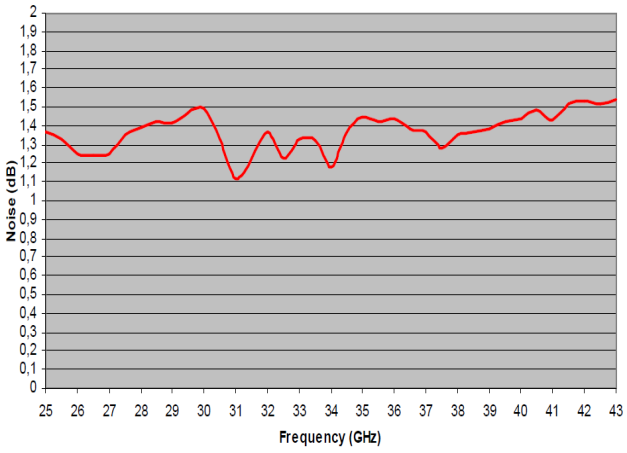
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



Noise Figure vs. Frequency



Application Information

A recommended module layout is proposed below. In the reference design, RF input and output are using coplanar transmission lines, microstrip transmission lines can also be used with similar performances. Due to the very high frequency, all path lengths and physical sizes of components should be minimized.

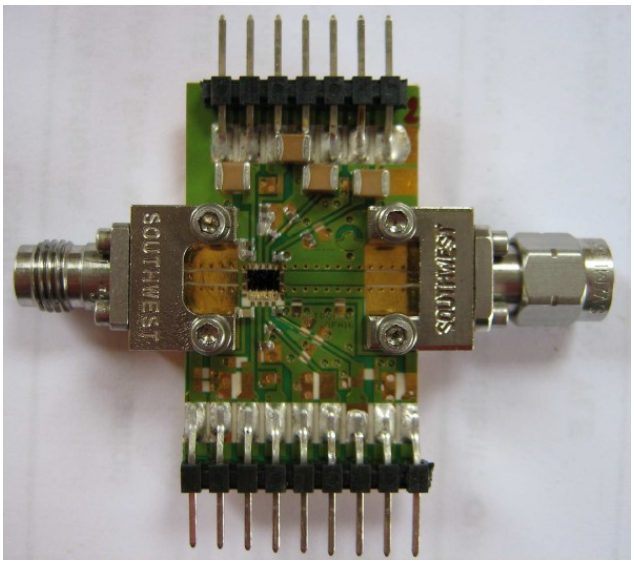
Both RF input and output bonding inductances should be minimized to give the best performance. Overall wire length should be kept as short as possible to reduce parasitic inductance. Degradation of gain and match will be evident at higher RF input and output inductances. Ribbon bonding technique can also be used.

All others bonding inductances (pads VD1, VD2, VD3, VD4, and VG1, VG2, VG3, VG4) should be kept as short as possible.

Decoupling chip capacitors 47 pF and Surface Mount Devices capacitors of 100 nF can be used to improve the power supply rejection and prevent unwanted inside and outside bandpath oscillations.

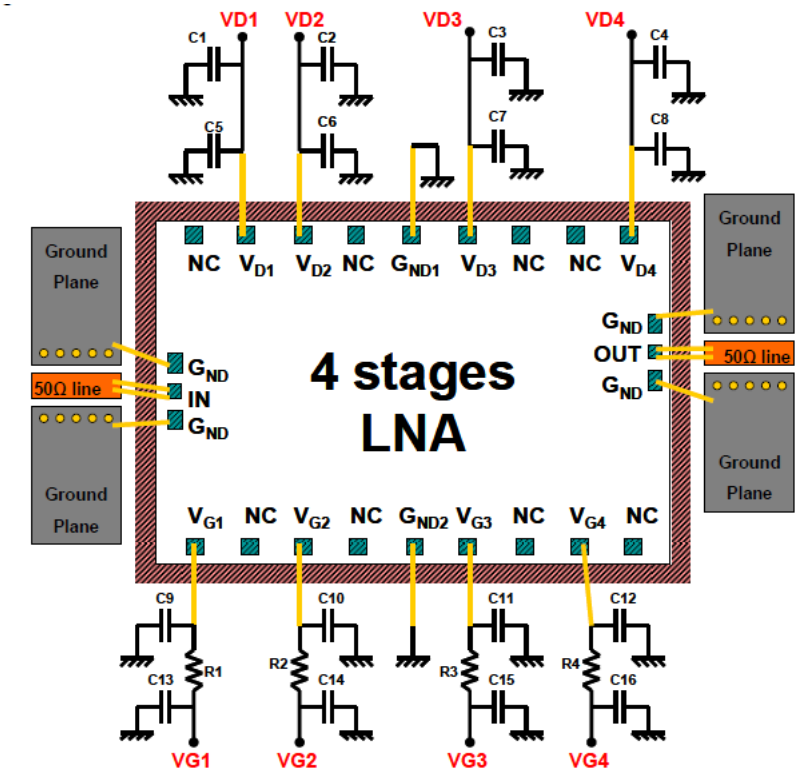
The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is key to use an uninterrupted ground plane. AuSn solder or silver conductive epoxy material can be used for capacitors and die attach.

The reference board is using Southwest removable millimeter wave connectors.



Application Layout

The layout of the decoupling capacitor are shown below, it can be noticed that drain and gates are carefully decoupled. Bonds between die pads and chip capacitors should be kept as short as possible reducing the equivalent inductance. A 47 pF chip capacitor is connected to each DC pad, it is also recommended to insert a second row of 100 nF CMS capacitor in cascade on gates and drain supply connections. The capacitors present on gates can form with a series resistor a low-pass filter slowing down the activation in case of grid control.



Parts List

Pad	X Coordinate
C1 - C4, C13 - C16	100 nF SMD Capacitor
C5 - C12	47 pF Chip Capacitor
R1 - R4	1 kΩ Resistor

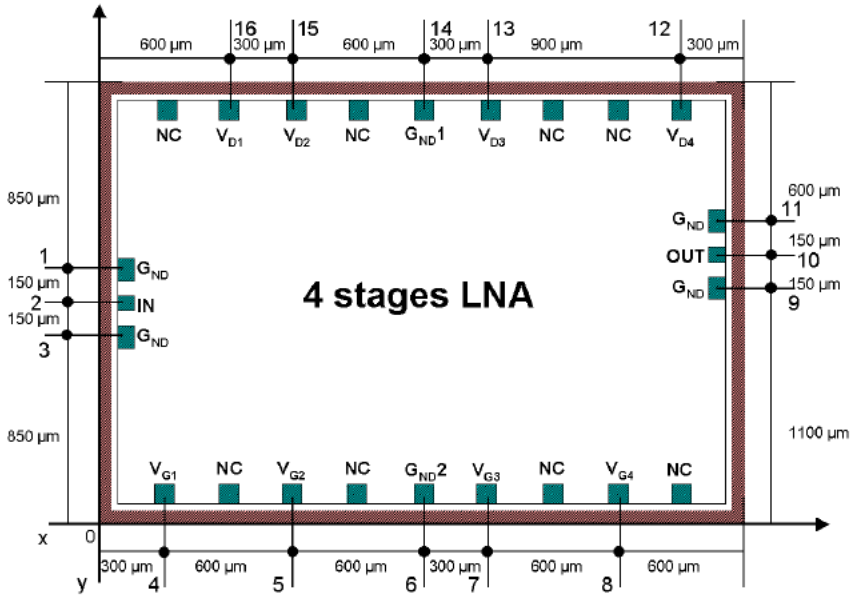
Soldering

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn.

Toxic fumes will be generated at temperatures higher than 400°C.

Bonding Pad Coordinates



The amplifier has a North and South face, North is top and South is bottom when RF input is on the left and RF output on the right.