Features

- Suitable for 10.7 Gb/s Optical Fiber Links
- Single Supply Voltage: +5 V
- Single-Ended Transimpedance:
  2.6 kΩ (68.5 dBΩ)
- Sensitivity: -22 dBm
- Built in AGC Function
- Consumption Current: 83 mA @ +5 V
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space and MIL-STD also Available
- RoHS* Compliant

Applications

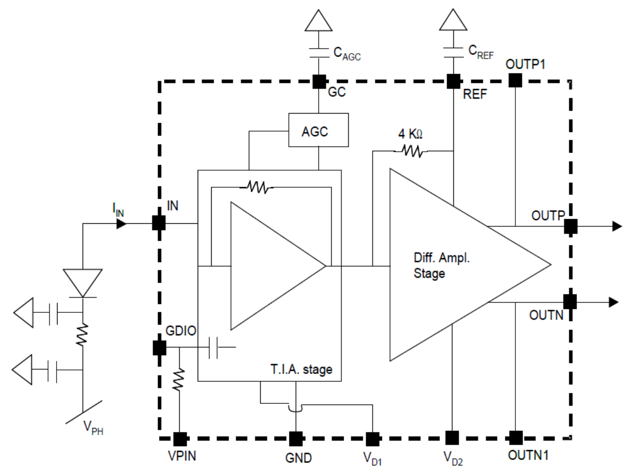
- 10 Gb/s Receivers Optical Sub Assemblies (ROSA)
- Optical Communications Network :SONET/SDH (OC-192/STM-64)
- Transponders modules : MSA300, XENPAK,XPAK, X2, XFP

Description

The CGY2116UH/C1 is a 10.7 Gb/s low noise transimpedance amplifier (TIA), designed for use in optical reception systems. The device can be used with a PIN or APD photodetector. The built-in AGC function enables the device to achieve more than 2.5 mApp as input overload current. The CGY2116UH/C1 features differential outputs and operates using a single 5 V supply voltage.

The die is manufactured using the 0.18 µm gate length pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2116UH/C1	10.7 Gb/s transimpedance amplifier

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

AC Characteristics[1-5]:

All measured data are at V_{DD} = 5 V; T_A = 25°C; R_L = 50 Ω. The TIA is measured on-wafer using RF probes without any light beam on the top of the IC (see note 1). Unless otherwise stated.
C_{PH} = 0.2 pF, L_{PH} = 0.5 nH, R_{PH} = 8 Ω, Freq. = 15 GHz, Inductance = 0.5 nH

Parameter	Conditions	Units	Min.	Typ.	Max.
Low Frequency Transimpedance Gain[1] @ 0.2 GHz, Single Ended	— V_{DD} = 3.3 V ±0.3 V, T_A = -40°C to +100°C V_{DD} = 5.0 V, T_A = +25°C	dBΩ	65.0	68.5	71.0
Transimpedance Ripple	0.2 MHz - 2.5 GHz 2.5 GHz - 4.0 GHz 4.0 GHz - 7.5 GHz 7.5 GHz - F_C	dB	-1.5 -1.5 -1.5 -3.0	-0.7 -1.0 ±1.0 —	+1.0 +1.0 +4.0 +3.0
Transimpedance Cut-Off Frequency	$\|ZT\| = \|ZT\|_{LF} - 3$ dB	GHz	8.5	9.6	—
Low Frequency Cut-Off	AC Coupled at All Outputs (via 100 nF Capacitor)	KHz	—	—	25
Maximum Peak Input Current	Before Input Overload	mApp	2.5	—	—
Group Delay	0.2 MHz - F_C	ps	—	±23	±35
Output Swing	Single Ended	mVpp	—	380	—
Output Reflection Coefficient	0.2 GHz - 5.5 GHz 5.5 GHz - 10.0 GHz	dB	—	-8.5 -11.5	-7 —
Total integrated input RMS noise	0.1 GHz - F_C	nA	—	800	—
Optical Input Sensitivity	ρ = 0.95 A/W, re = 12 dB, BER = 10^{-12}	dBm	—	-21.7	—
Output Load Termination	OUTN, OUTP	Ω	—	50	—

1. The gain specification is guaranteed down to the lower cut-off frequency, 0.2 GHz is specified as a reference for convenience of measurement.
2. The CGY2116UH/C1 is AC coupled at its outputs via an external capacitor, C. So the low frequency cut-off is determined by the time constant RC, where R is the total output resistance (on-chip output series 50 Ω impedance of the TIA circuit plus the external 50 Ω load) equivalent to 100 Ω. Assuming that C is 100 nF, the low frequency cut-off is given by : Fc_low = 1/(2*pi*R*C) = 16 KHz.
3. This characteristic is guaranteed by design and verified by measurement (using evaluation boards with 231 – 1 PRBS, BER of 10-12).
4. With typical output bond wire inductances LOUTP, LOUTN = 0.5 nH, the Output reflection coefficient is improved.
5. The sensitivity is computed from the total integrated input RMS noise. To obtain a system bit-error rate of 10^{-12}, the signal-to-noise ratio must be 14.1 or better. The input sensitivity, expressed in average power, is calculated as:

$$Sensitivity = 10\log\left(\frac{14.1\times I_{NOISE}\times(r_e+1)}{2\times\rho\times(r_e-1)}\times 1000\right) \text{ dBm}$$

where ρ and r_e are respectively, the photodiode responsivity in A/W and the extinction ratio. I_{NOISE} is measured in amperes.

DC Characteristics:

Minimum/Maximum values are defined at V_{DD} = 5 V, T_A = +25°C (unless otherwise stated)

Parameter	Units	Min.	Typ.	Max.
Supply Current	mA	—	83	110
DC Input Voltage	V	—	1.3	1.4
Input Average Current for AGC Activation	µA	—	100	—
Voltage Offset Between the 2 Outputs in Absolute Value	V	—	0	+0.8
DC Voltage Available @ OUTP & OUTN Pads	V	—	4.40	4.75

VINDC: DC voltage available at the RF input pad of the TIA.
For an input average current less than IIN_LIM, the output voltage is proportional to the input current. Whereas for an input average current higher than IIN_LIM, the AGC function is activated, leading to a linear decrease of the gain.

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Supply Voltage	-0.5 V to +8.0 V
Photodiode Biasing Voltage	-15 V to +15 V
Input Average Photo Current @ 5.0 V	50 mA
Junction Temperature	+150°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

Operating Conditions

Parameter	Absolute Maximum
Positive Supply Voltage	+4.75 V to +5.25 V
Operating Temperature	-10°C to +85°C
Input Interface	DC Coupled
Output Interface	AC Coupled

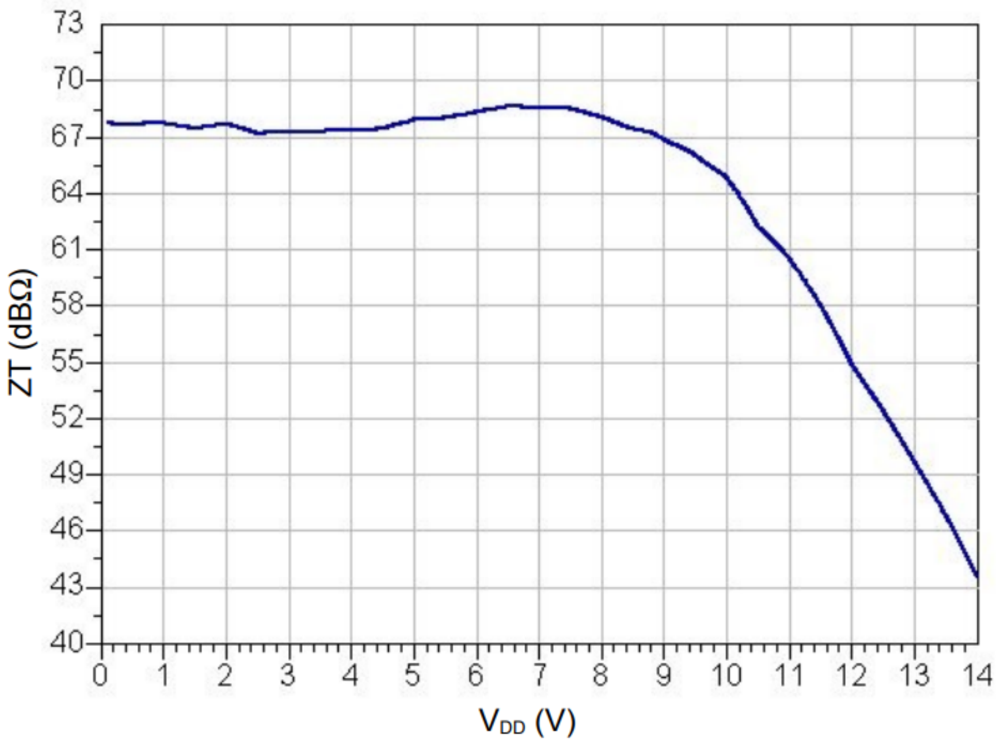
Handling Procedures

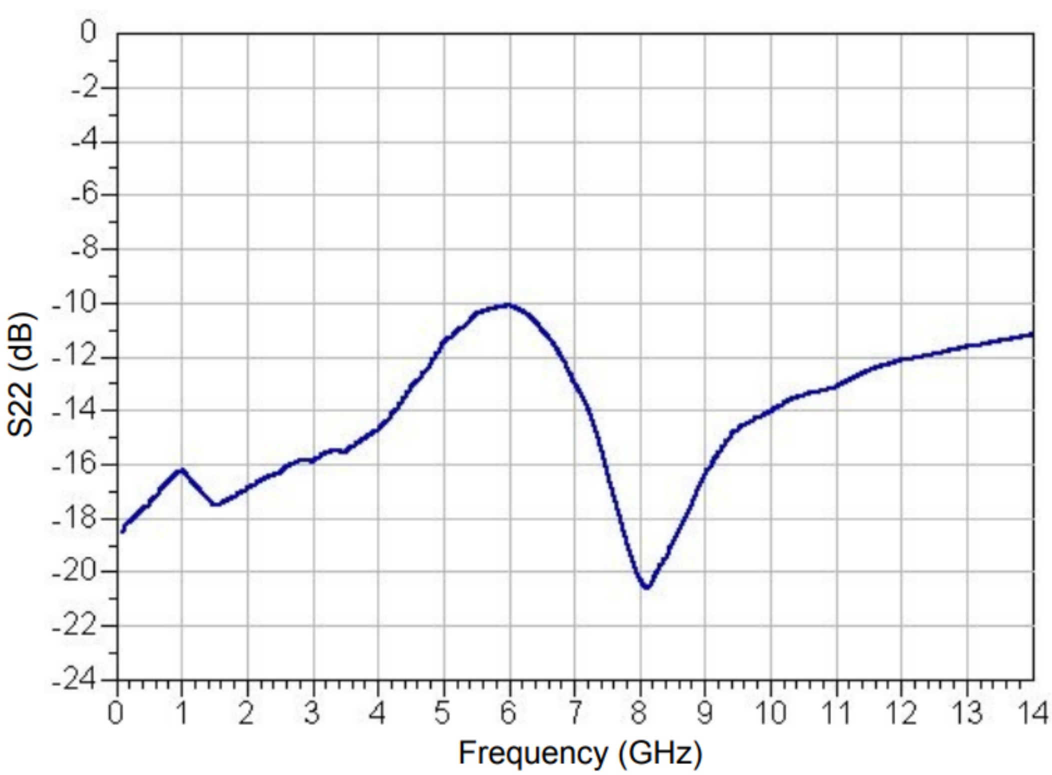
Please observe the following precautions to avoid damage:

Static Sensitivity

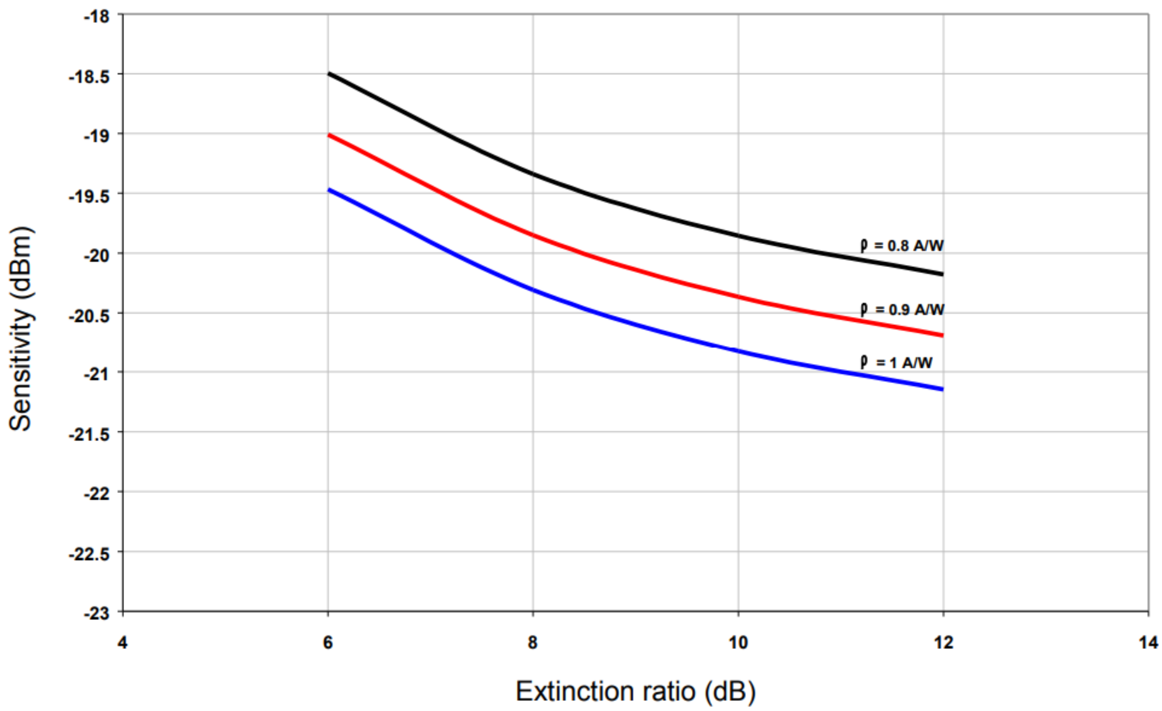
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

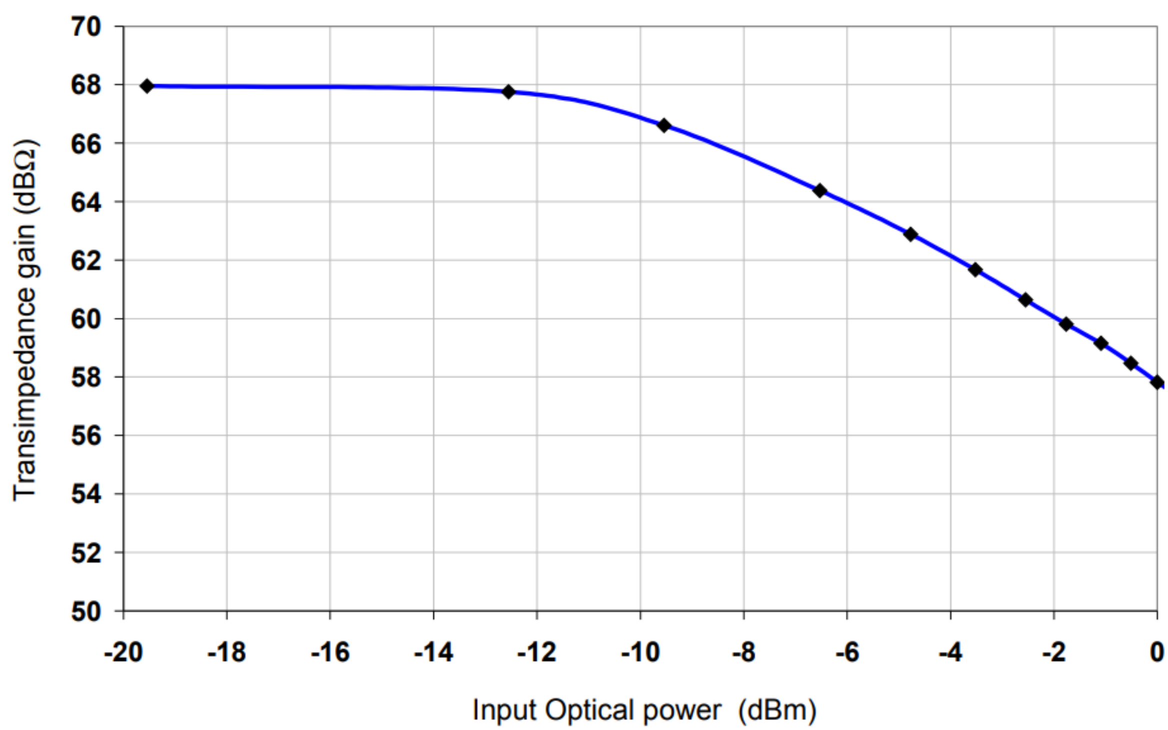
Typical Performance Curves:





Typical Performance Curves:



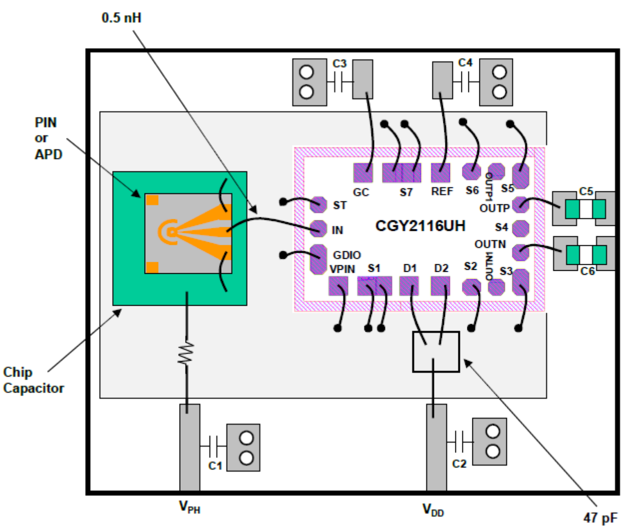


Single Ended Transimpedance gain at F = 200 MHz vs. input optical power

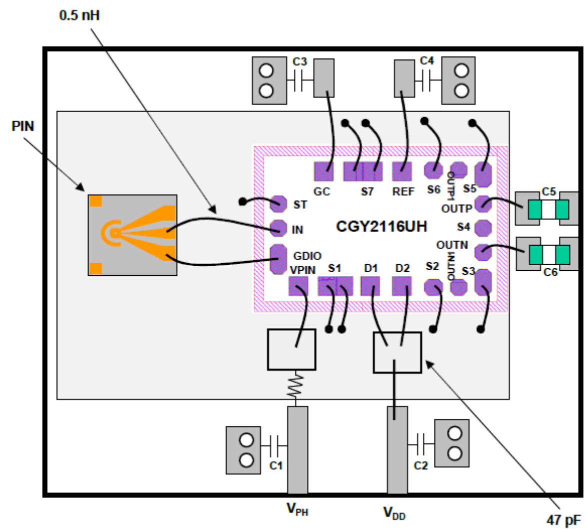
Bonding Diagram & Assembly Information

The performance of the photo-receiver module is dependent both on the photodiode capacitance and on the interconnection inductance between the photodiode and the CGY2116UH/C1. The circuit was optimized for a photodiode capacitance CPH lower than 0.2 pF with a low photodiode series resistance (RPH) to give the best noise performance from the receiver module.

In this application note, two modules layout are proposed, the difference occurs only at the receiver input:



suitable for both PIN and APD photodiodes



suitable only for a PIN photodiode

Recommended Parts List

Pad Name	Description	Manufacturer Part Number
C1, C2, C3, C4, C5, C6	100 nF	0402 sub-mount capacitors
C1, C2, C3, C4	100 nF	GMA085F51A104ZD01T (size: 0.8 x 0.8 x 0.5 mm) or chip capacitors from Murata
C1, C2, C3, C4	100 nF	VL3030Y5V104Z16VH5 (size: 0.8 x 0.8 x 0.56 mm) or VL4080X7R104M16VH5 (size: 1.016 x 2.032 x 0.635 mm) or chip capacitors from Presidio

The CGY2116UH/C1 also offers an option to bias the photodiode through the VPIN pad. It is important to note that APD photodiodes cannot be mounted with this configuration (more than 15 V, DC supply voltage (required for APD) cannot be applied on this pad due to potential problems via the substrate).

It is recommended to use a total input equivalent bonding inductance value of typical 0.5 nH, while 1 nH should be considered as a maximum value. The length of the output bonding wire should be minimized.

To improve power supply rejection throughout the frequency band, 47 pF and 100 nF capacitors are required. The 47 pF capacitor provides a decoupling at frequencies above 1 GHz and should be positioned close to the chip. The 100 nF capacitor is for decoupling at lower frequencies and can be positioned further away from the chip.

A good RF grounding connection should be maintained between the ground pads of the chip and the ground of the system. The grounding of high gain amplifiers is critical for achieving the maximum microwave performance. Inductance due to bonding wires can cause unwanted feedback, performance degradation, resonances and possibly oscillations. To reduce the inductance effect, several bond wires can be used in parallel on each bond pad.

The CGY2116UH/C1 can be used in differential or single ended topology. In the case of single ended configuration, the unused output pad is connected to a 50 Ω load via a 100 nF DC blocking capacitor.

Power Supply Sequence :

The following power supply sequence is recommended (VPH : Photodiode bias, VDD : TIA bias):

a) Always turn on the photodiode bias VPH first or simultaneously with VDD. Since the photodiode is direct coupled to the TIA input, powering VDD first can damage the photodiode through forward bias and excess current.
b) Apply the input optical signal.

It is important to apply the DC voltage from ground, then increases them to their desired values.

Handling Precautions :

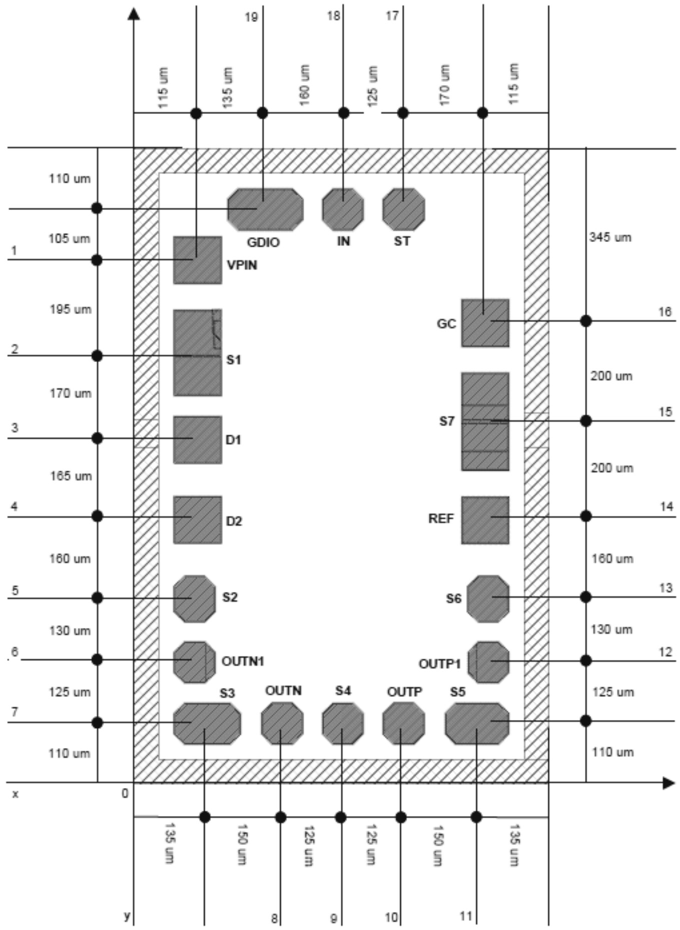
a) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
b) Require all handling personal to wear a conductive bracelet or wrist-strap connected to the ground.
c) Ground all test equipment and all soldering iron tops.
d) Store IC’s and other devices such as chip capacitors in their conductive carriers until they are soldered.

Pad Position

Pad #	Pad Name	Coordinate		Description
		X	Y	
1	VPIN	1055	115	Photodiode DC supply voltage pad
2	S1	860	115	bond to ground
3	D1	690	115	First stage DC supply voltage, must be decoupled to ground using an external capacitor
4	D2	525	115	Second stage DC supply voltage, must be decoupled to ground using an external capacitor
5	S2	365	115	bond to ground
6	OUTN1	235	115	RF inverted output (recommended for TO-can package)
7	S3	110	135	bond to ground
8	OUTN	110	285	RF inverted output
9	S4	110	410	bond to ground
10	OUTP	110	535	RF non-inverted output
11	S5	110	685	bond to ground
12	OUTP1	235	705	RF non-inverted output (recommended for TO-can package)
13	S6	365	705	bond to ground
14	REF	525	705	Reference input voltage, must be decoupled to ground using an external capacitor
15	S&	725	705	bond to ground
16	GC	925	705	Gain control pad, must be decoupled to ground using an external capacitor
17	ST	1160	535	bond to ground
18	IN	1160	410	RF input, connected to the photodiode anode
19	GDIO	1160	250	connected to the photodiode cathode

X=0, Y=0 at bottom left corner.
Co-ordinates correspond to the center of the bonding pad.
See Mechanical Information for more details.

Mechanical Information



Chip Size: 1270 x 820 µm (±15 µm)
VPIN, D1, D2, GC, REF: 100 x 100 µm
IN, ST, OUTP, OUTP1, OUTN, OUTN!, S4: 88 x 88 µm
S2, S6: 88 x 98 µm
S3, S5: 88 x 140 µm
S1: 100 x 180 µm
S7: 100 x 200 µm
Substrate Thickness: 200 µm