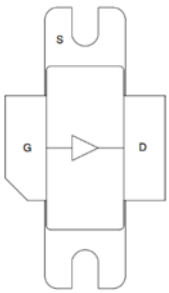
850 W GaN Amplifier
1.2 - 1.4 GHz

CGHV14800F1
Rev. V1

Features

- Saturated Power: 850 W
- Large Signal Gain: 14 dB
- Drain Efficiency: 65%
- Long Pulse Operation
- RoHS* Compliant



Applications

- Avionics - TACAN, DME, IFF
- L-Band Radar
- General Purpose Amplification

Description

The CGHV14800F1 is an 850 W packaged, partially-matched transistor utilizing the high performance, 0.4 µm GaN on SiC production process. This device operates up to 1.4 GHz and supports both defense and commercial related avionics and radar applications. The CGHV14800F1 typically achieves 850 W of saturated output power with 14 dB of large signal gain and 65% drain efficiency via a 1.2 - 1.4 GHz reference design.

Packaged in a thermally-enhanced, flange package, the CGHV14800F1 provides superior performance under long pulse operation allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Pin Description

Pin	Description
D	Drain
G	Gate
S	Source

Ordering Information

Part Number	Package
CGHV14800F1	bulk
CGHV14800F1-AMP	test board

Typical Performance: Freq: 1.2 - 1.4 GHz, T_C = +25°C

Parameter	1.2 GHz	1.3 GHz	1.4 GHz	Units
Small Signal Gain[1,2]	18.1	17.7	17.8	dB
Power Gain[1,3]	14.1	14.0	13.8	dB
Output Power[1,3]	59.1	58.9	58.8	dBm
Drain Efficiency[1,3]	70.0	68.6	67.2	%

1. V_{DD} = 50 V, I_{DQ} = 800 mA.
2. Measured @ P_{IN} = -20 dBm.
3. Measured @ P_{IN} = +45 dBm and 2 ms; Duty Cycle = 20%.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Recommended Operating Conditions

Parameter	Conditions	Units	Typ.
Input Power	Pulsed only	dBm	45
Drain Voltage	V_{DS} = 10 V, I_D = 83.6 mA	V	50
Gate Voltage	V_{DS} = 50 V, I_D = 500 mA	V	-2.95
Drain Current	V_{DS} = 6 V, V_{GS} = 2 V	mA	800
Case Temperature	—	°C	-40 to 85

RF Specifications (CGHV14800F1-AMP) [4]

V_{DD} = 50 V, I_{DQ} = 800 mA, PW = 100 µs, DC = 5%, T_B = 25 °C (unless otherwise noted)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Output Power	P_{IN} = 45 dBm 1.2 GHz 1.4 GHz	W	 850 820	 920 994	 1060 1340
Drain Efficiency	P_{IN} = 45 dBm 1.2 GHz 1.4 GHz	%	 67 65	 70.9 72.4	 78 86
Power Gain	P_{IN} = 45 dBm 1.2 GHz 1.4 GHz	dB	 14.2 14.1	 14.6 14.9	 15.3 16.7
Small-Signal Gain	—	dB	—	18	—
Input Return Loss	—	dB	—	12	—
Output Return Loss	—	dB	—	5	—

4. Final testing and screening for all transistor sales is performed using the CGHV14800F1-AMP at 1.2-1.4 GHz.

Absolute Maximum Ratings (Not Simultaneous)[5,6]

Parameter	Absolute Maximum
Input Power	47 dBm
Drain Source Voltage	50 V
Gate Source Voltage	-10 V to +2 V
Drain Current	24 A
Gate Current	133 mA
Dissipated Power	545 W @ +85 °C, 2 ms / 20%
Storage Temperature	-65°C to +150°C
Mounting Temperature	260°C @ 30 seconds
Junction Temperature	225°C @ MTTF > 1E6
Output Mismatch Stress	5:1
Pulse Width/Duty Cycle	2000 µs / 20% @ +85°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.

Thermal Characteristics

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Operating Junction Temperature	Freq = 1.4 GHz, V_D = 50 V, I_{DQ} = 800 mA, I_{DRIVE} = 23 A , P_{IN} = 45 dBm, P_{OUT} = 58.6 dBm, P_{DISS} = 433 W, T_C = 85°C, PW = 2 ms, DC = 20%	°C	—	198	—
Thermal Resistance ($R_{\theta JC}$)		°C/W	—	0.26	—

Bias Sequencing

Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of -5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

1. Turn RF off
2. Apply pinch-off voltage to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

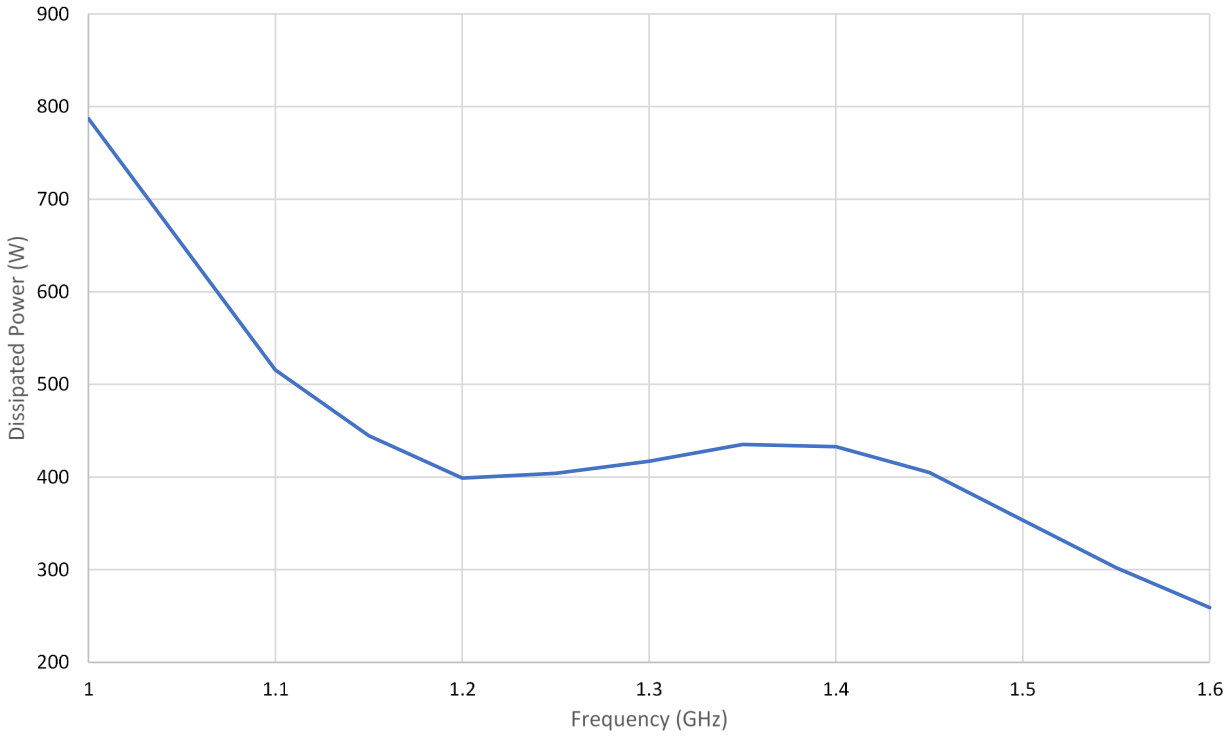
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B and CDM Class 0CB devices.

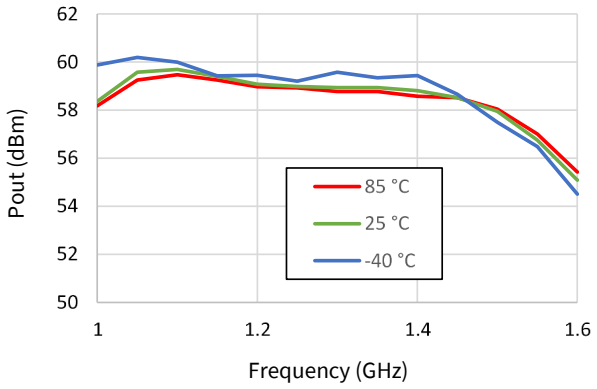
Power Dissipation v. Frequency (Tcase = 85°C)



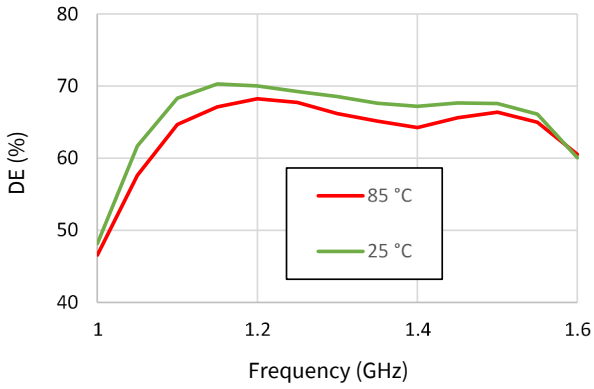
Typical Performance Curves:

Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency

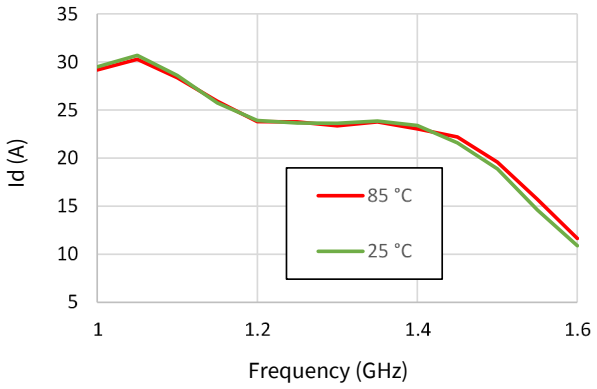
Pout v. Frequency v. Temperature



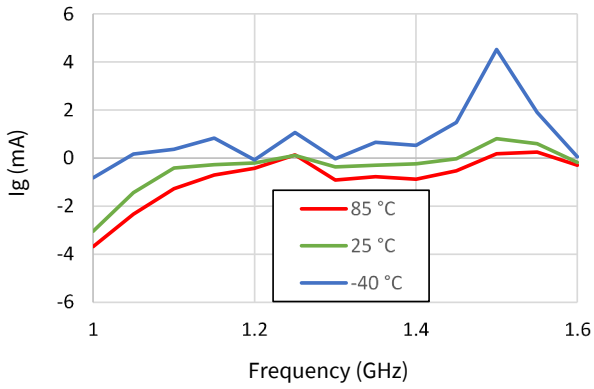
DE v. Frequency v. Temperature



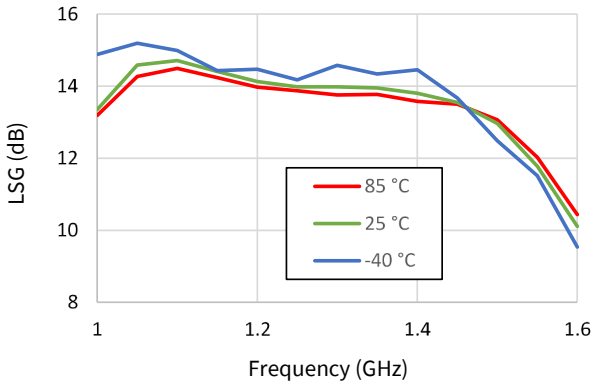
Id v. Frequency v. Temperature



Ig v. Frequency v. Temperature



LSG v. Frequency v. Temperature



Typical Performance Curves:

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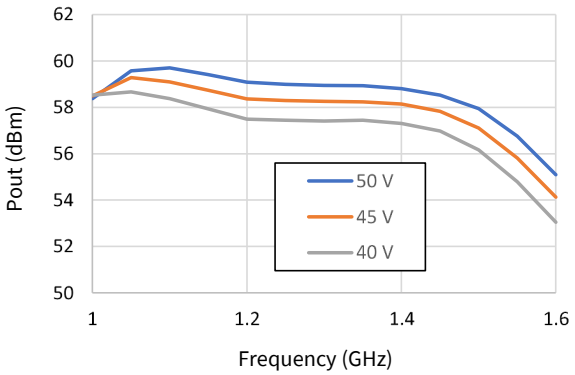
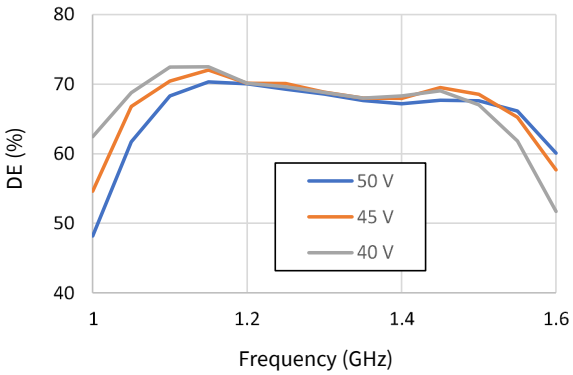
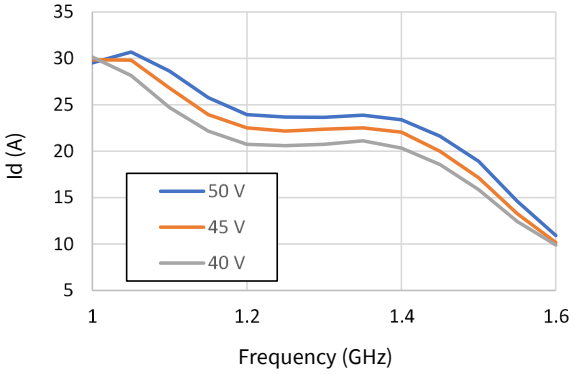
Pout v. Frequency v. Vd



DE v. Frequency v. Vd



Id v. Frequency v. Vd



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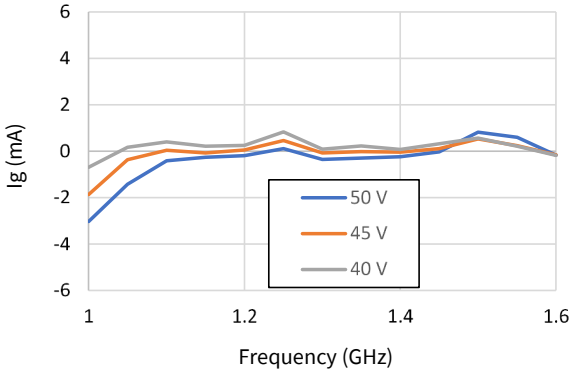

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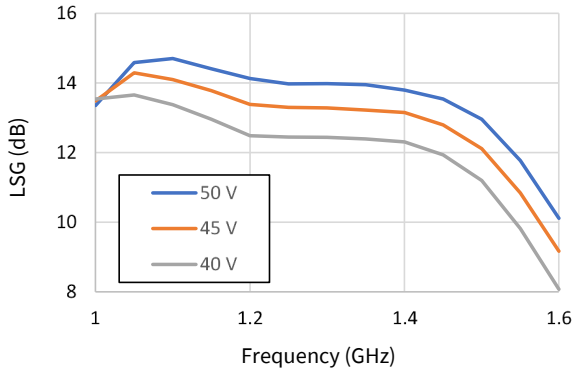

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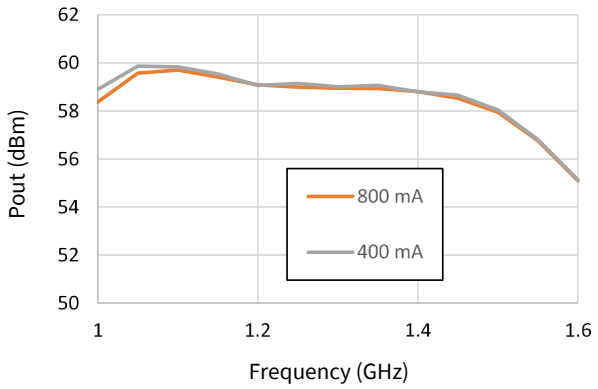
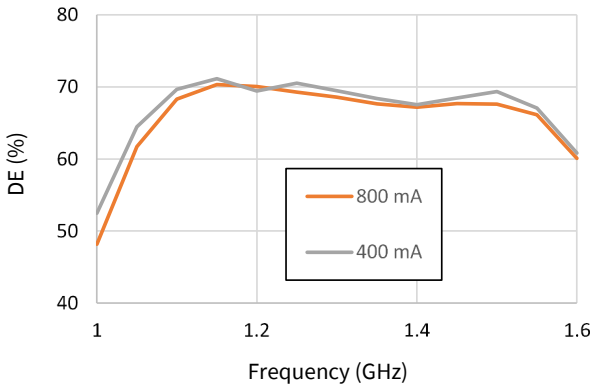
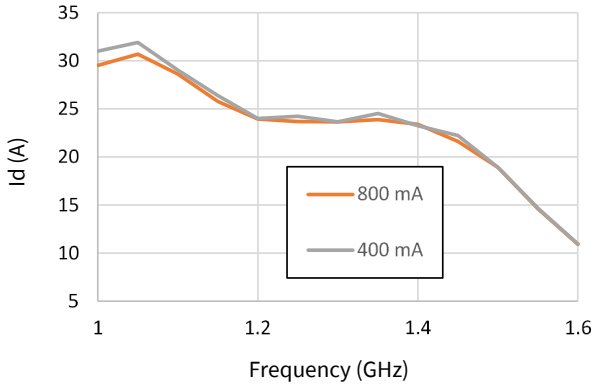
Pout v. Frequency v. Idq



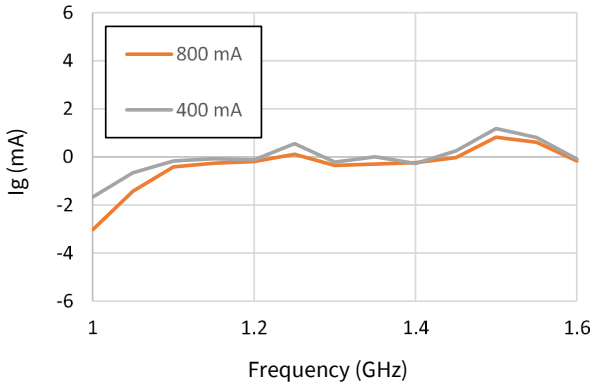
DE v. Frequency v. Idq



Id v. Frequency v. Idq



Ig v. Frequency v. Idq



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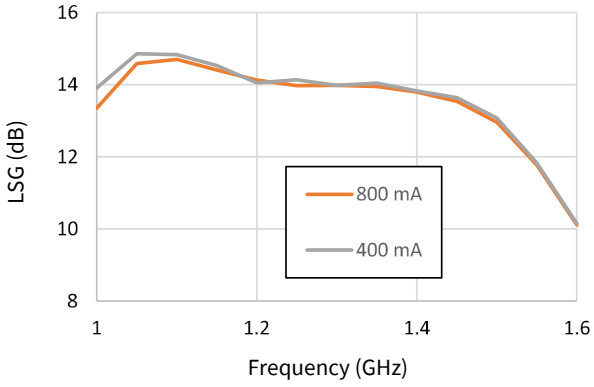

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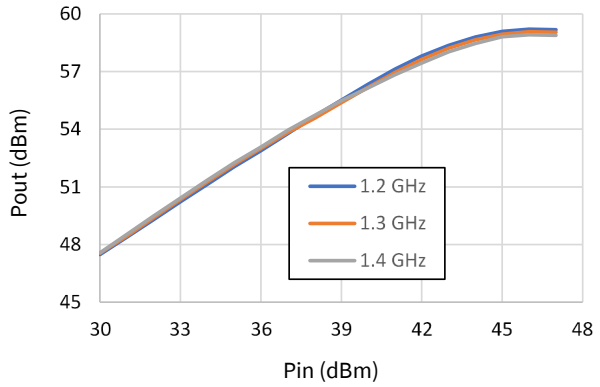
Pout v. Pin v. Frequency



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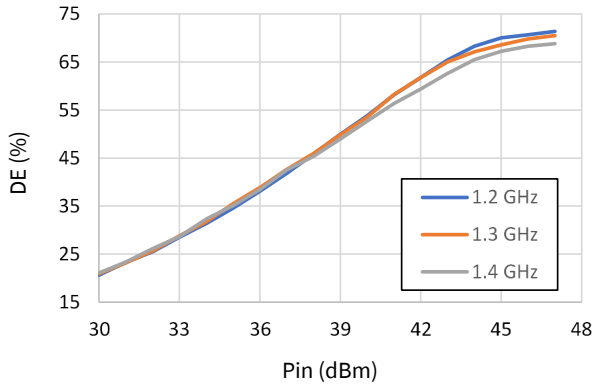

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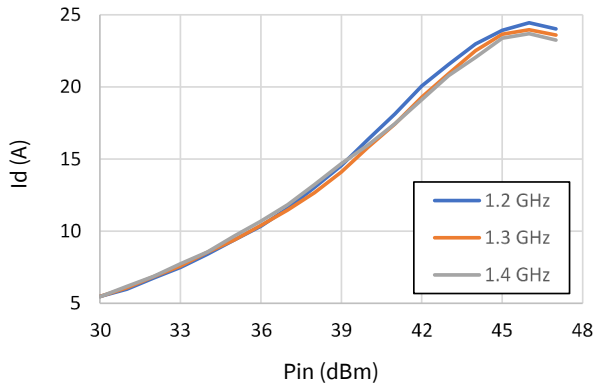
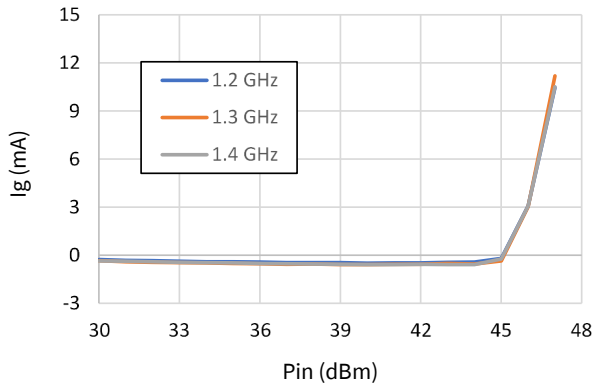
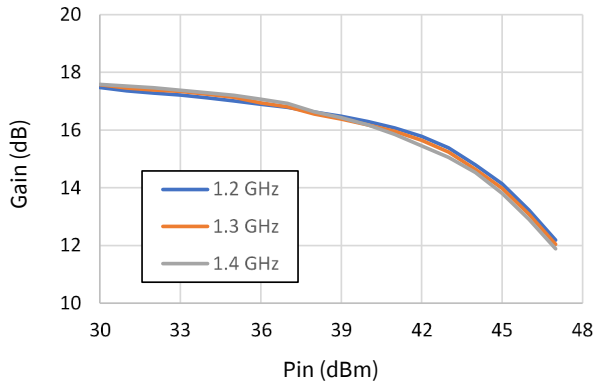


Ig v. Pin v. Frequency



Gain v. Pin v. Frequency



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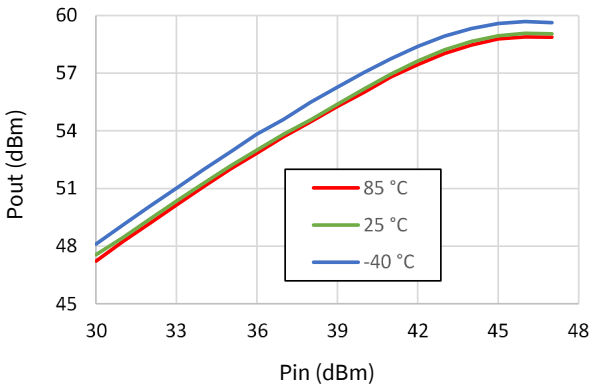
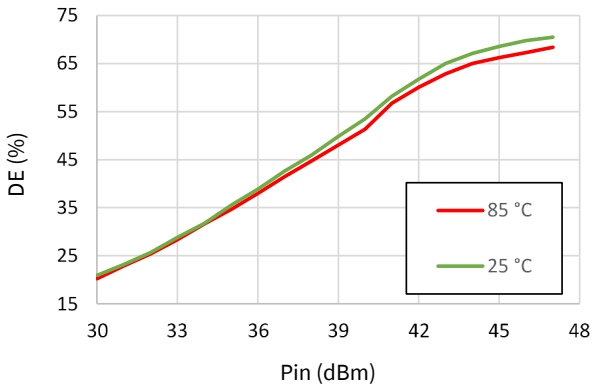
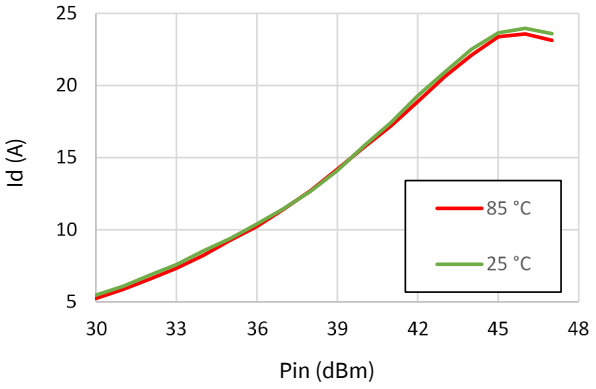
Pout v. Pin v. Temperature



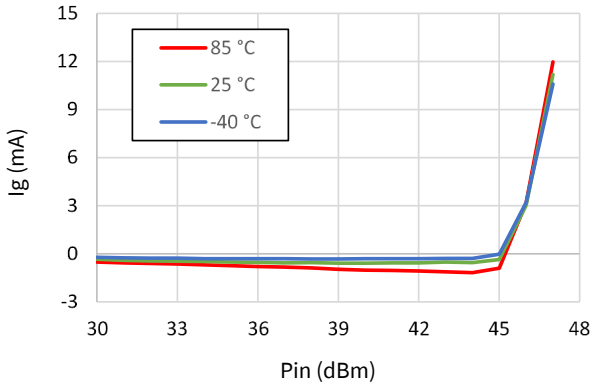
DE v. Pin v. Temperature



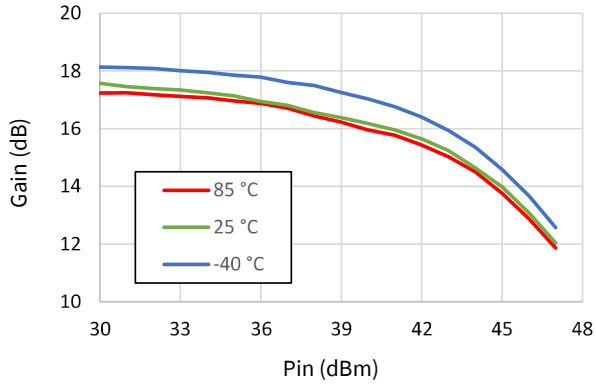
Id v. Pin v. Temperature



Ig v. Pin v. Temperature



Gain v. Pin v. Temperature



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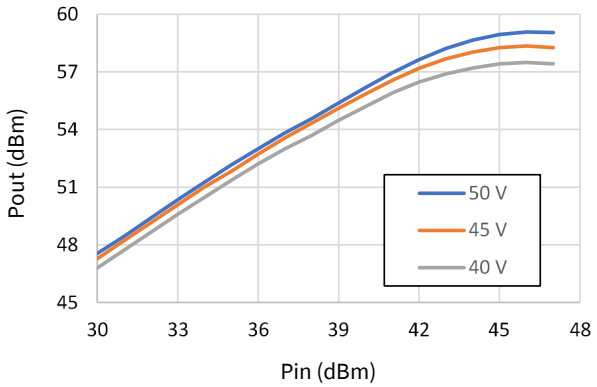
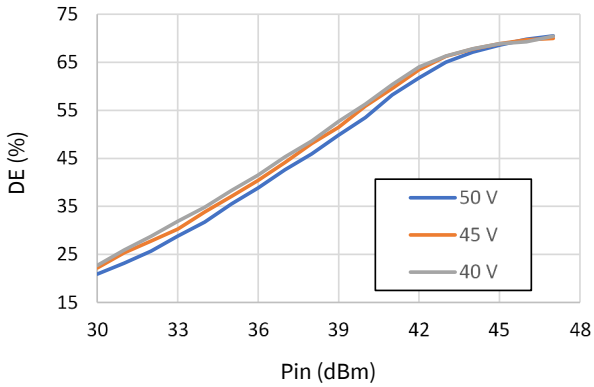
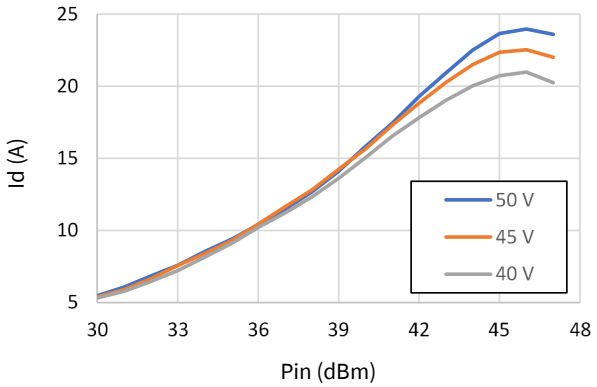
Pout v. Pin v. Vd



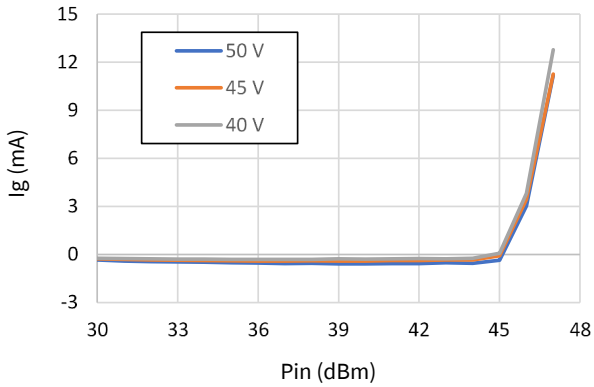
DE v. Pin v. Vd



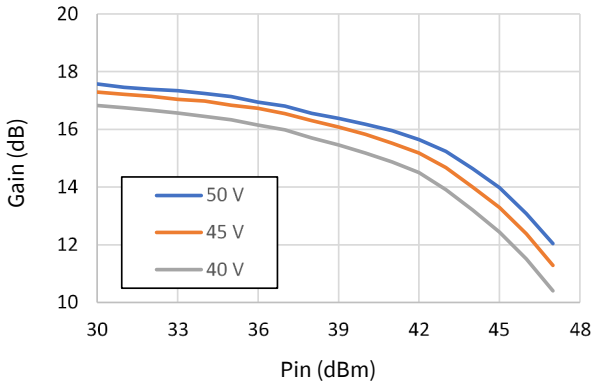
Id v. Pin v. Vd



Ig v. Pin v. Vd



Gain v. Pin v. Vd



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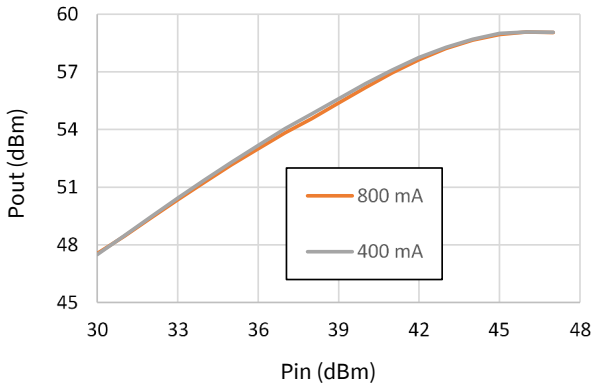
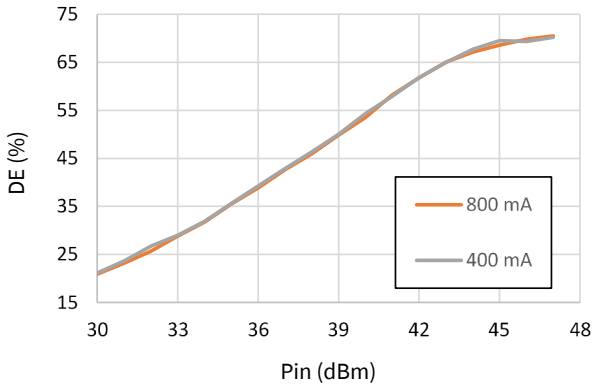
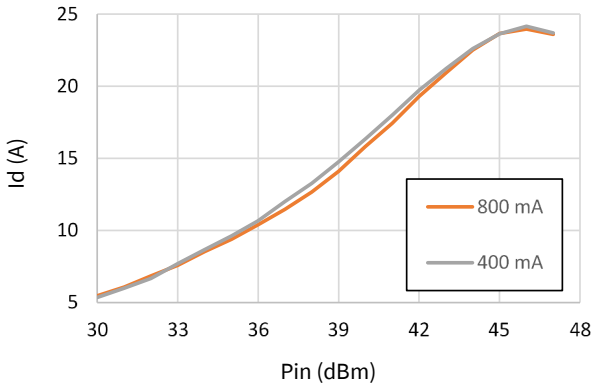
Pout v. Pin v. Idq



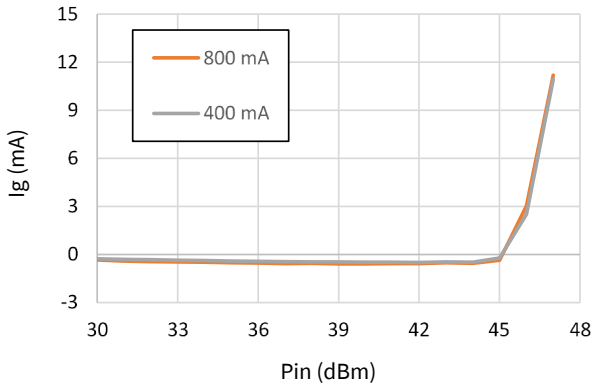
DE v. Pin v. Idq



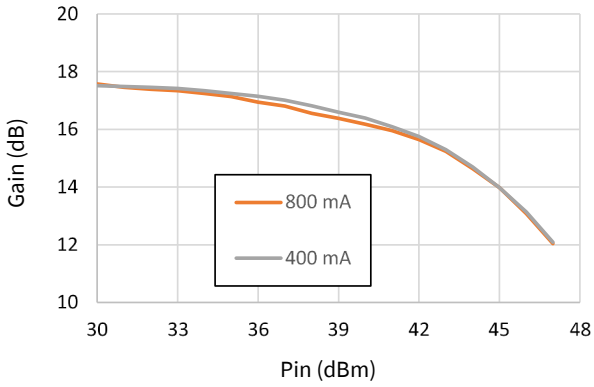
Id v. Pin v. Idq



Ig v. Pin v. Idq



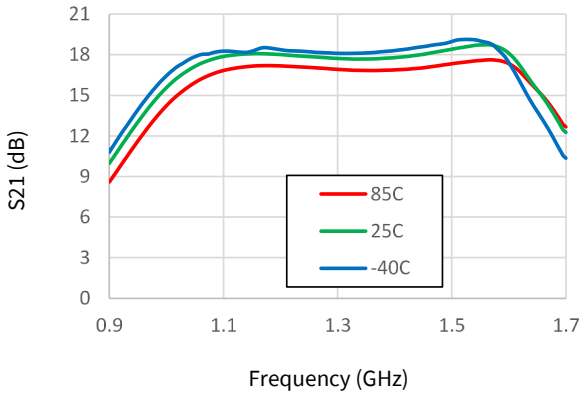
Gain v. Pin v. Idq



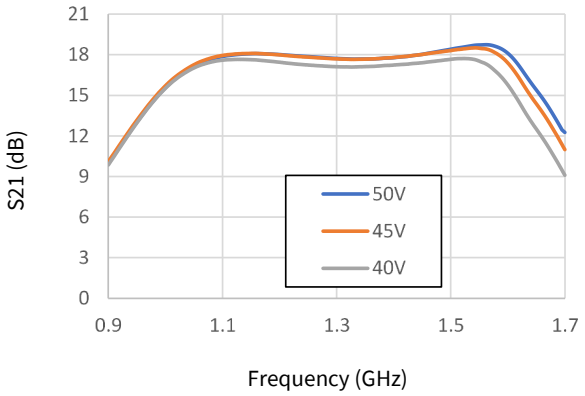
Typical Performance Curves:

Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency

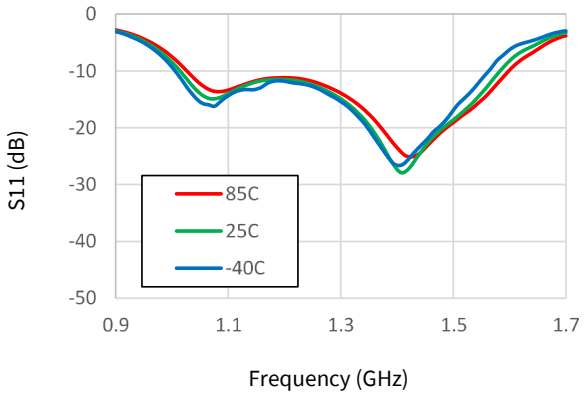
S21 v. Frequency v. Temperature



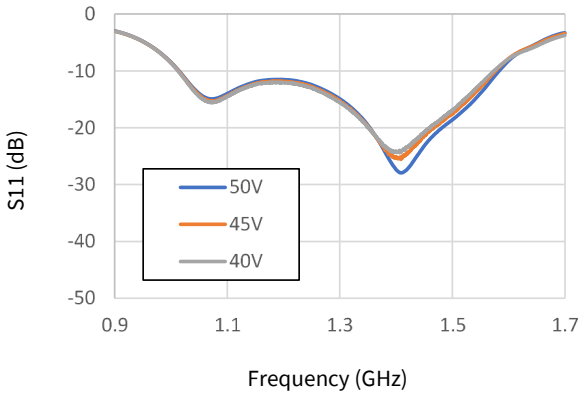
S21 v. Frequency v. Vd



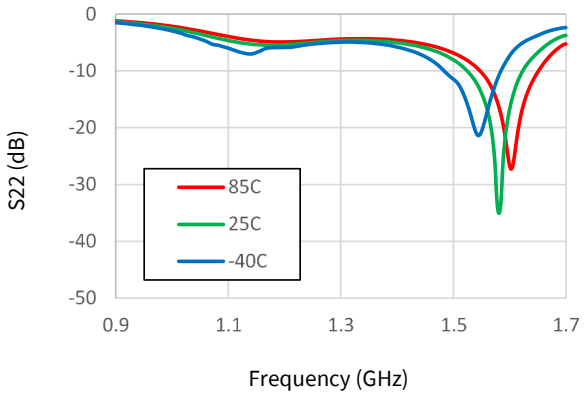
S11 v. Frequency v. Temperature



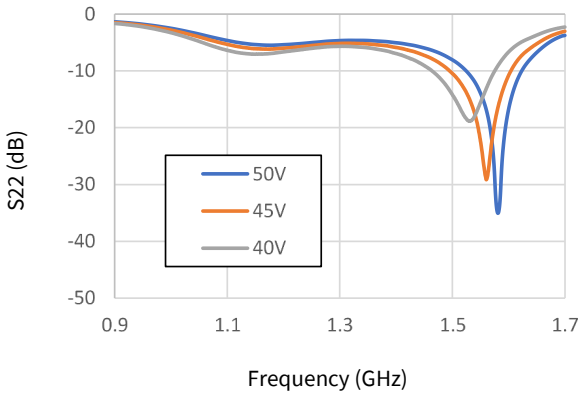
S11 v. Frequency v. Vd



S22 v. Frequency v. Temperature



S22 v. Frequency v. Vd



Typical Performance Curves:

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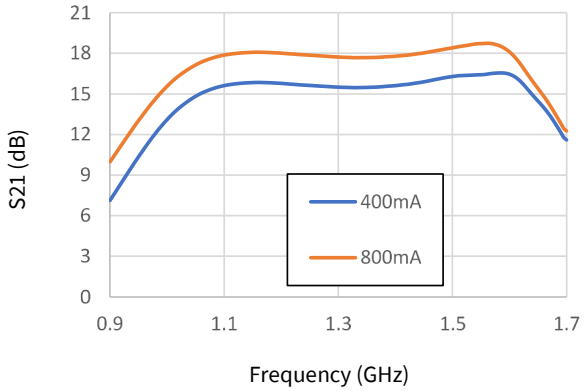
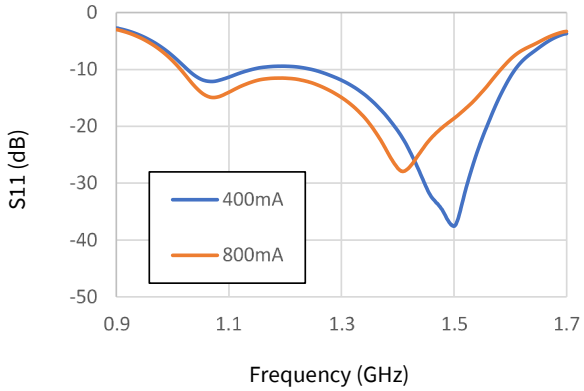
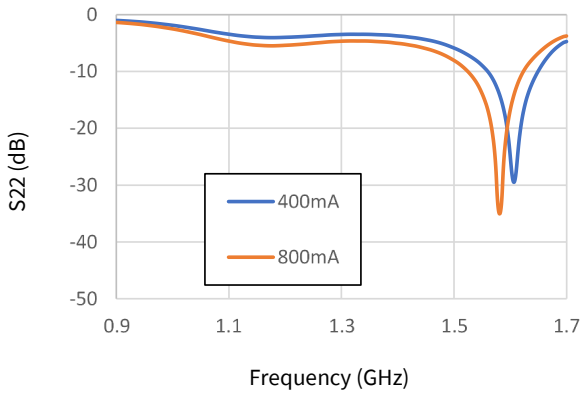
S21 v. Frequency v. Idq



S11 v. Frequency v. Idq



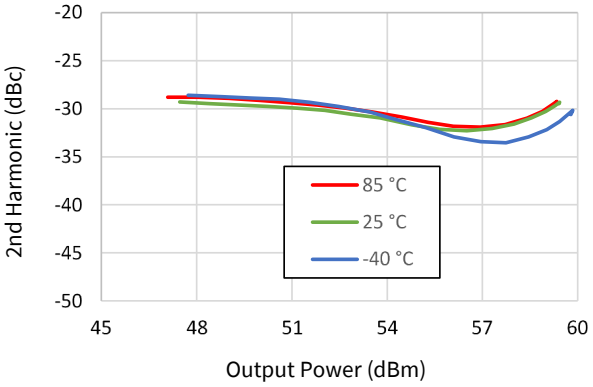
S22 v. Frequency v. Idq



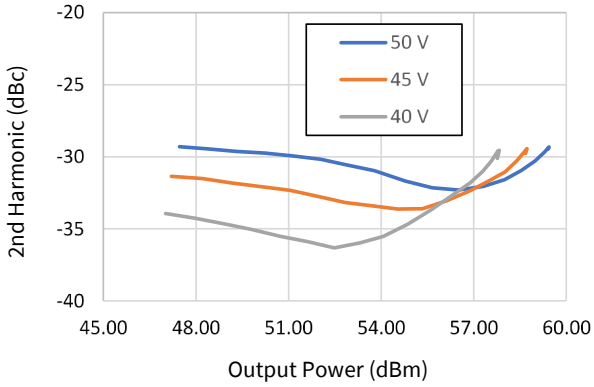
Typical Performance Curves:

Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency

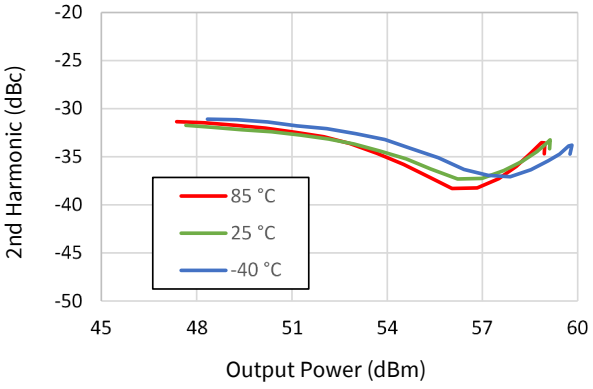
f/2 v. Pout v. Temperature, F1



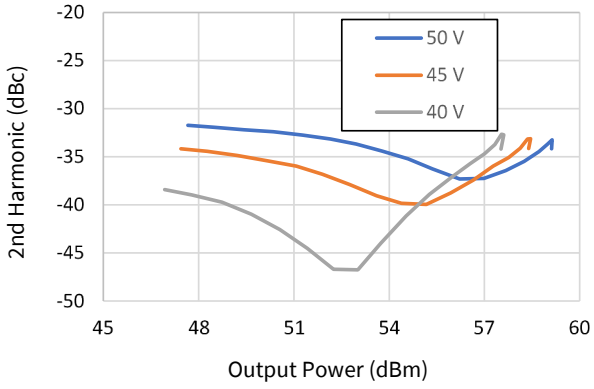
f/2 v. Pout v. Vd, F1



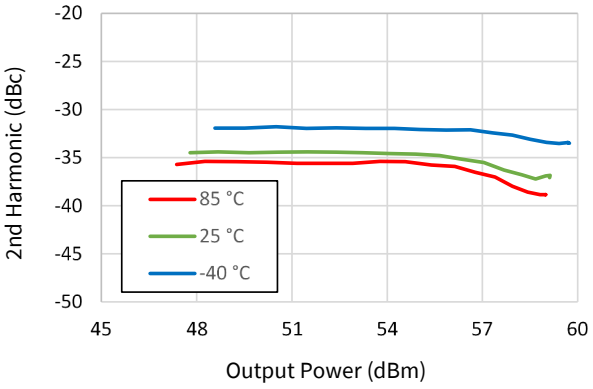
f/2 v. Pout v. Temperature, F2



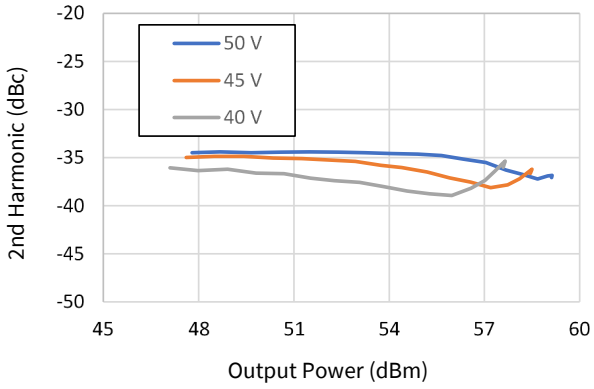
f/2 v. Pout v. Vd, F2



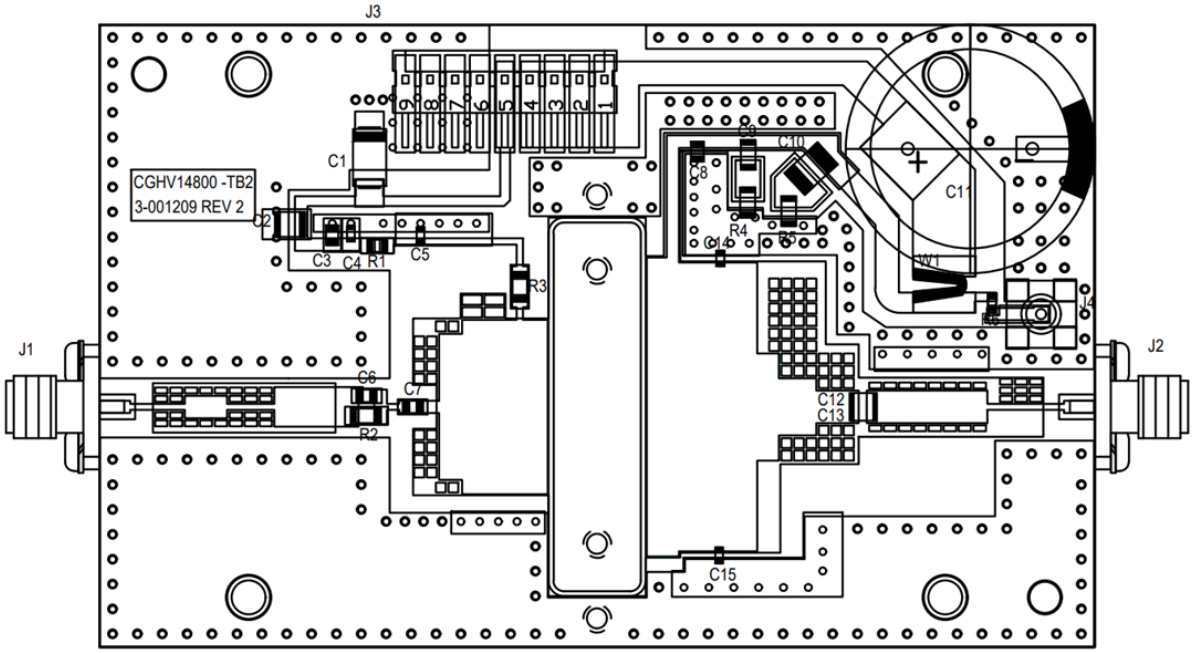
f/2 v. Pout v. Temperature, F3



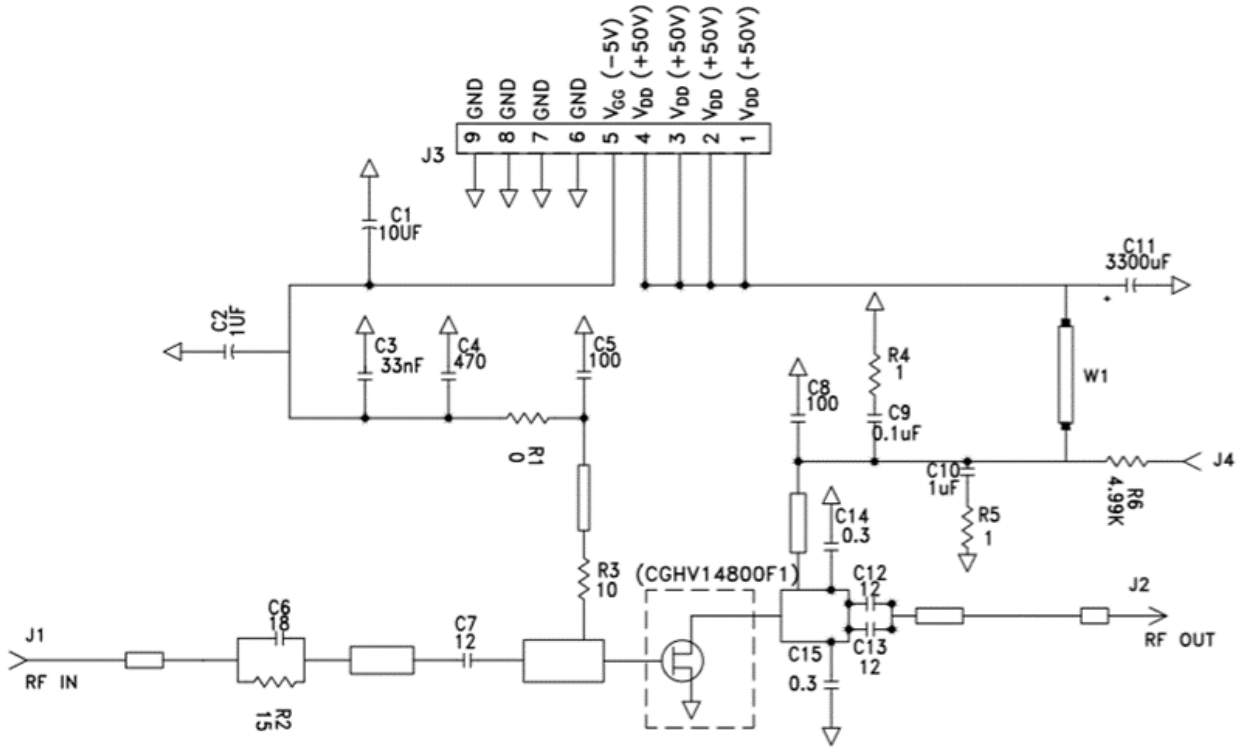
f/2 v. Pout v. Vd, F3



Assembly Drawing



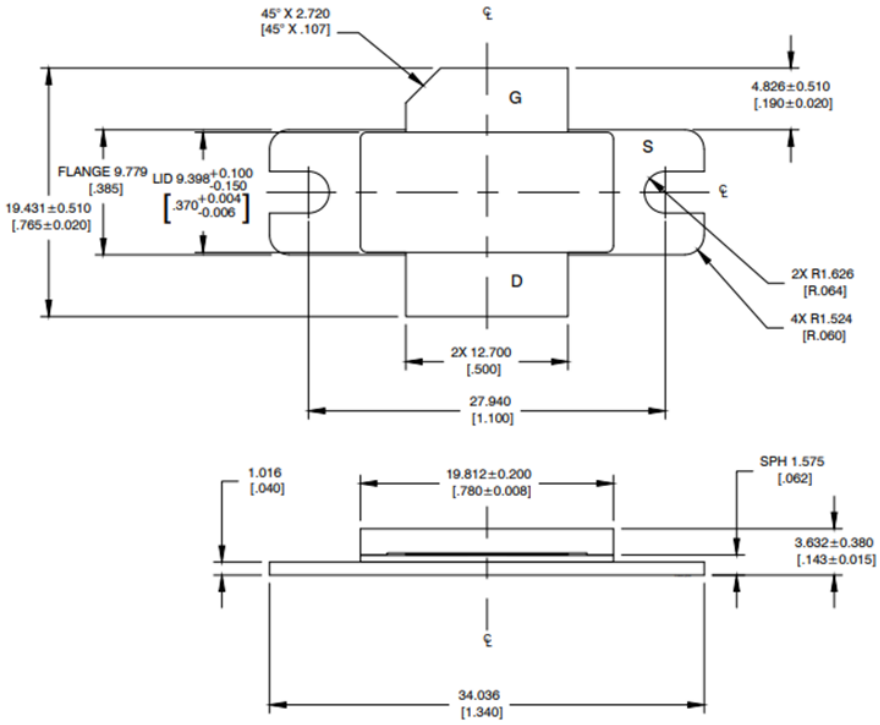
Application Circuit Schematic



Parts List

Reference Designator	Description	Qty
C1	CAP, 10 µF 16V TANTALUM	1
C2, C10	CAP, 1 µF, 100V, 10%, X7R, 1210	2
C3	CAP, 33000 pF, 0805,100V, X7R	1
C4	CAP, 470 pF, 0805, 100V, C0G	1
C5, C8	CAP, 100 pF, +/-5%, 250V, 0805, ATC 600F	2
C6	CAP, 18 pF, +/-5%, 250V, 0603, ATC 600S	1
C7	CAP, 12 pF, +/- 5%, 250V, 0805, ATC 600F	1
C9	CAP, 0.1 µF, +/- 10%, 100V, 1206, 1206	1
C11	CAP, 3300 µF, +/-20%, 100V, ELECTROLYTIC	1
C12, C13	CAP, 12 pF, +/- 2%,500V, ATC800B	2
C14, C15	CAP, 0.3 pF, +/- 0.05pF, 0603, ATC	2
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
R1	RES, 0 Ω, 1/8W, 1206, 5%	1
R2	RES, 15 Ω, 1/8W, 1206, 5%	1
R3	RES, 10 Ω, 1/8W, 1206, 5%	1
R4,R5	RES, 1 Ω, 1/8W, 1206, 5%	2
R6	RES, 4.99 kΩ, 1/16W,0603,1%	1
W1	CABLE ,18 AWG, 4.2”	1
	PCB, Rogers 3010, 0.025” THK, CGHV14800 1.2-1.4GHZ	1
	BASEPLATE, COPPER, 4.00 X 2.50 X 0.49, ALTERNATE HOLE PATTERN	1
	2-56 SOC HD SCREW 1/4 SS	4
	#2 SPLIT LOCKWASHER SS	4
	Indium Foil in channel (0.0002" thick)	1

Product Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. PINS: D=DRAIN
   S=SOURCE (FLANGE)
   G=GATE
3. LEAD THICKNESS: $0.10^{+0.051}_{-0.025}$ [$.004^{+.002}_{-.001}$]
4. PLATING (GOLD TOP LAYER): 1.14 ± 0.38 MICRON [45 ± 15 MICROINCH].
5. THE CONTENTS OF THIS DRAWING ARE INTENDED TO REPRESENT THE PRODUCT IN MARKETING GRAPHICS ONLY, AND NOT INTENDED TO BE USED FOR ANY PRODUCTION OR INTERNAL QUALIFICATION PURPOSE.

Pin #	Description
1	Gate / RFIN
2	Drain / RFOUT
3	Source / Flange