M08028/M08038 SD, HD, 3G Cable Driver

The M08028/M08038 are high-speed, low-power, low-jitter cable drivers designed to drive serial digital video data through 75 Ω coaxial cable. The M08038 cable driver is optimized for performance from 143 Mbps up to 2970 Mbps. The M08028 cable driver is optimized for performance from 143 Mbps up to 1485 Mbps. They have selectable slew rates for SD-SDI and HD-SDI applications.

The typical output rise/fall time of the M08028/M08038 is 100 ps for HD and 3G rates. It has a typical set slew rate of 600 ps at SD rates. The M08028/M08038 support a maximum single ended output swing of 1600 mVpp, when configured appropriately.

The M08028/M08038 are packaged in a 4x4 mm QFN package to simplify the PCB and reduce package parasitics with resulting improvements in Output Return Loss (ORL). It is available in an RoHS compliant package, that is backwards compatible with standard JEDEC SnPb processes.

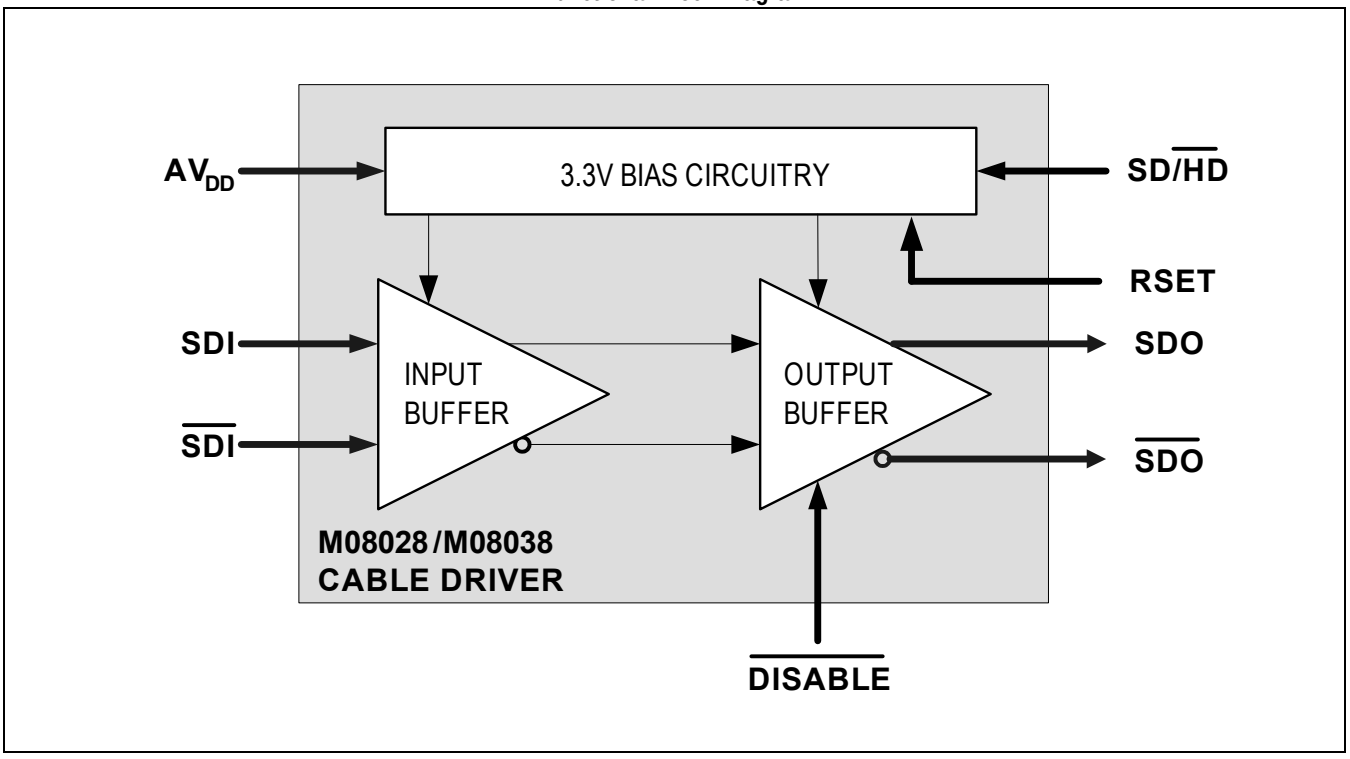
Features

- 3G, HD, SD operation for M08038
- HD, SD operation for M08028
- 800 mVpp single ended output swing (typical)
- 1600 mVpp maximum single ended output swing
- SD/HD slew rate control
- 3.3 V supply
- Low P_{TOTAL} (144 mW @ 3.3 V)
- Small form factor (4x4 mm, 16-pin QFN package)
- RoHS compliant
- Output disable

Applications

- Surveillance/CCTV Cameras
- Industrial and Professional Cameras
- Digital Video Recorders (DVR)
- Video Mixers and Switchers
- Digital Image Transmitter Devices
- Distribution Amplifiers
- Repeaters

Functional Block Diagram



Ordering Information

Part Number	Data Rates Supported	Package	Operating Temperature
M08028G-11*	143–1485 Mbps	4x4 mm QFN, 16-pin (RoHS compliant)	-10 °C to 85 °C
M08038G-11*	143–2970 Mbps	4x4 mm QFN, 16-pin (RoHS compliant)	-10 °C to 85 °C

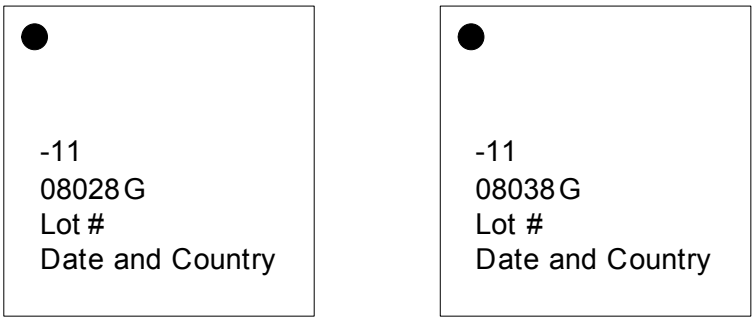
NOTES:

* The letter 'G' designator after the part number indicates a RoHS-compliant package. Refer to www.mindspeed.com for additional information.

Revision History

Revision	Level	Date	Description
A	Release	May 2011	Initial Release.

M08028/M08038 Marking Diagrams



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
AV_{DD}	Power	AV_{SS} - 0.5	AV_{SS} + 3.47	V
$V_{MAX, IO}$	Maximum/minimum input/output voltage on any input/output pin	AV_{SS} - 0.5	AV_{DD} + 0.5	V
T_{STORE}	Storage Temperature	-65	+150	°C
$V_{ESD, HBM}$	Human Body Model	2000	—	V
$V_{ESD, CDM}$	Charge Device Model	500	—	V

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
AV_{DD}	Power	3.13	3.3	3.46	V
AV_{SS}	Ground	—	0	—	V
T_{AMB}	Ambient Temperature	-10	—	+85	°C
θ_{JA}	Junction to ambient Thermal Resistance	—	61	—	°C/W
AV_{TERM}	75 Ω Output Termination Voltage	See Table 3-1			

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Typical	Maximum	Units
I_{DD}	Supply Current	1, 2	27	36	mA
I_{TERM}	Current in external termination resistors	1, 2	22	—	mA
P_{TOTAL}	Total on-chip power dissipation (AV_{DD} = 3.3 V, AV_{DDTERM} = 3.3 V)	1, 2, 3	144	—	mW
P_{TOTAL}	Total on-chip power dissipation (AV_{DD} = 3.3 V, AV_{DDTERM} = 5.0 V)	1, 2, 3	181	—	mW

NOTES:

1. Recommended operating conditions—see Table 1-2.
2. 800 mVpp output swing, terminated as in Figure 3-3.
3. Does not include off-chip power dissipated by termination resistors.

Table 1-4. CMOS Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	AV_{DD}	V
V_{IL}	Input Logic Low Voltage	1	0	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic High)	1	-100	100	µA
I_{IL}	Input Current (logic Low)	1	-100	100	µA

NOTE:

1. Specified at recommended operating condition—see Table 1-2.

Table 1-5. High-Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input Bit Rate (M08028)	1, 2	0	—	1485	Mbps
DR_{IN}	Input Bit Rate (M08038)	1, 2	0	—	2970	Mbps
V_{IN}	Differential input swing	1, 3, 4	100	—	2000	mV_{PPD}
V_{ICM}	Input Common-Mode Voltage	1	1200	—	3.3	mV
V_{IH}	Maximum Input High Voltage	1	—	—	3.7	V
V_{IL}	Minimum Input Low Voltage	1	1.2	—	—	V
R_{IN}	Single-ended input impedance	1	—	13.33	20	kΩ

NOTES:

1. Specified at recommended operation conditions—see Table 1-2.
2. Part is DC coupled at the input.
3. Example 1200 mV_{PPD} = 600 mV_{PP} single-ended.
4. Minimum input level defined as BER ≤ 10^{-12}.

Table 1-6. High-Speed Output Electrical Specifications (M08028)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output bit rates	1, 5	0	—	1485	Mbps
t_R/t_F	SD rise/fall time (20-80%)	1, 3, 5	400	600	800	ps
	HD rise/fall time (20-80%)	1, 3, 5	—	100	135	ps
$t_R/t_F\ \Delta$	Rise/fall mismatch (SD rate)	1, 2, 5	—	40	100	ps
	Rise/fall mismatch (HD rate)	1, 2, 5	—	10	30	ps
$V_{OUT, SE}$	Single-ended voltage swing	1, 2, 4, 5	500	800	1600	mVpp
$V_{PP, TOL}$	Swing level variation at 800 mVpp [RSET = 750 Ω ± 1%] (single-ended)	1, 2, 3, 5	-7	—	7	%
$V_{OVER/UNDER}$	Overshoot/undershoot	1, 2, 5	-10	—	10	%
t_{JIT}	Additive output jitter (SD rate)	1, 5, 8	—	40	60	ps
	Additive output jitter (HD rate)	1, 5, 8	—	20	30	ps

Table 1-6. High-Speed Output Electrical Specifications (M08028)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DCD_{DATA}	Duty Cycle Distortion (SD rate)	1, 2, 5, 6, 8	—	20	70	ps
	Duty Cycle Distortion (HD rate)	1, 2, 5, 6, 8	—	15	30	ps
S22	Output Return Loss (5 MHz to 1.5 GHz)	1, 2, 5, 7	15	—	—	dB

NOTES:

1. Entire table specified at recommended operating condition with 400 mV_{PPD} input—see Table 1-2.
2. Specification verified at 800 mV_{PP} output with 1 m cable on MSPD test board. System results may vary.
3. Rated at 800 mV_{PP} output swing (using a 750 Ω ±1% resistor at RSET).
4. Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
5. Into 75 Ω back termination and 75 Ω load and appropriate external termination voltage, see Table 3-1, Figure 3-3.
6. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
7. Measured under DC conditions that simulate AC coupling, **V_T = 3.3 V**.
8. Measured using a “1010” data pattern.

Table 1-7. High-Speed Output Electrical Specifications (M08038)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output bit rates	1, 5	0	—	2970	Mbps
t_R/t_F	SD rise/fall time (20-80%)	1, 3, 5	400	600	800	ps
	HD/3G rise/fall time (20-80%)	1, 3, 5	—	100	135	ps
t_R/t_F Δ	Rise/fall mismatch (SD rate)	1, 2, 5	—	40	100	ps
	Rise/fall mismatch (HD/3G rate)	1, 2, 5	—	10	30	ps
$V_{OUT, SE}$	Single-ended voltage swing	1, 2, 4, 5	500	800	1600	mVpp
$V_{PP, TOL}$	Swing level output variation at 800 mVpp [RSET = 750 Ω ± 1%] (single-ended)	1, 2, 3, 5	-7	—	7	%
$V_{OVER/UNDER}$	Overshoot/undershoot	1, 2, 5	-10	—	10	%
t_{JIT}	Additive output jitter (SD rate)	1, 5, 8	—	40	60	ps
	Additive output jitter (HD/3G rate)	1, 5, 8	—	20	30	ps
DCD_{DATA}	Duty Cycle Distortion (SD rate)	1, 2, 5, 6, 8	—	20	70	ps
	Duty Cycle Distortion (HD/3G rate)	1, 2, 5, 6, 8	—	15	30	ps

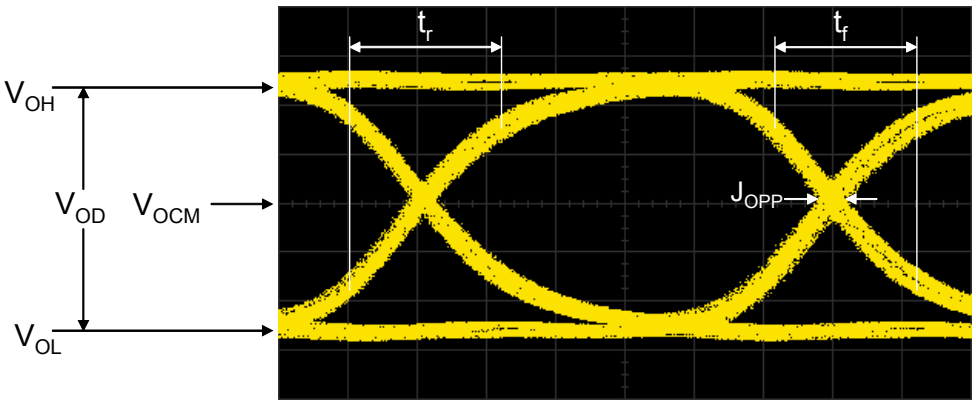
Table 1-7. High-Speed Output Electrical Specifications (M08038)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
S22	Output Return Loss (5 MHz to 1.5 GHz)	1, 2, 5, 7	15	—	—	dB
	Output Return Loss (1.5 GHz to 2.97 GHz)	1, 2, 5, 7	10	—	—	dB

NOTES:

1. Entire table specified at recommended operating condition with 400 mV_{PPD} input—see Table 1-2.
2. Specification verified at 800 mV_{PP} output with 1 m cable on MSPD test board. System results may vary.
3. Rated at 800 mV_{PP} output swing (using a 750 Ω ±1% resistor at RSET).
4. Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
5. Into 75 Ω back termination and 75 Ω load and appropriate external termination voltage, see Table 3-1, Figure 3-3.
6. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
7. Measured under DC conditions that simulate AC coupling, **V_T = 3.3 V**.
8. Measured using a “1010” data pattern.

Figure 1-1. Output Symbols Definition



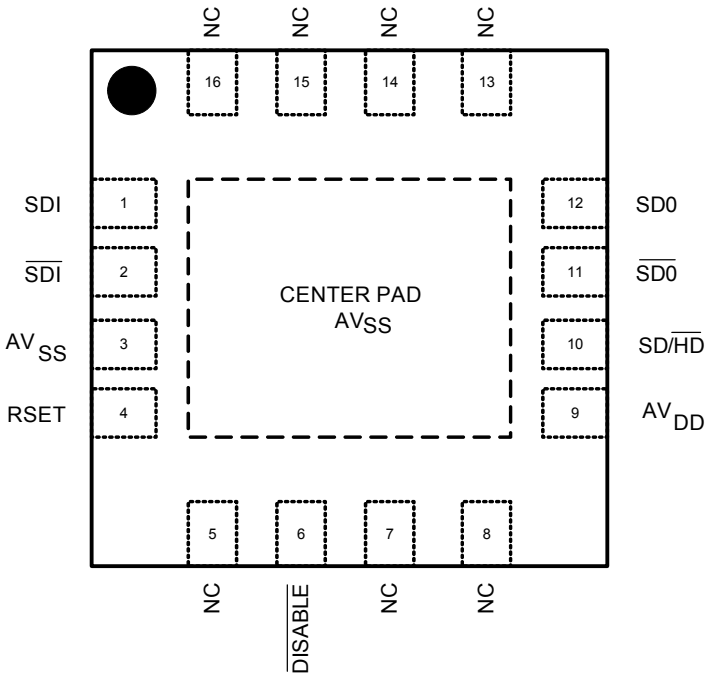
V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

2.0 Pinout Diagram, Pin Descriptions, and Package Outline Diagram

The M08028/M08038 are available in a 16-pin 4x4 mm QFN package. The pinout is shown in Figure 2-1 and the package drawing in Figure 2-2.

Figure 2-1. M08028/M08038 Pinout



Top View

Table 2-1. M08028/M08038 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	9	Power	Analog positive supply
AV_{SS}	3	Power	Ground
SDI/$\overline{SDI}$	1, 2	CML input	High-speed serial digital input
SDO/$\overline{SDO}$	12, 11	CML output	High-speed serial digital output
RSET	4	Analog input	Low-speed analog input
SD/$\overline{HD}$	10	CMOS input	Internal pull up
$\overline{DISABLE}$	6	CMOS input	Internal pull up
NC	5, 7, 8, 13, 14, 15, 16	No connect	Do not connect

2.1 M08028/M08038 Signals by Interface Group

Table 2-2. Interface Pins

Pin Name	Pin #	Function	Default	Type
RSET	4	Input control signal for setting the single-ended output swing amplitude. Higher output swing levels or reduced variations with a ±1% tolerance external resistor. For 800 mVpp single-ended, a 750 Ω ±1% resistor to AV_{DD} is recommended.	—	Analog Input

Table 2-3. Power Pins

Pin Name	Pin #	Function	Type
AV_{SS}	3	Ground	Power
AV_{DD}	9	Analog Positive Supply	Power
NC	5, 7, 8, 13, 14, 15, 16	Do not connect.	N/A
Center Pad	—	Ground	Power

Table 2-4. High-speed Signal Pins

Pin Name	Pin #	Function	Default	Type
SDI/$\overline{SDI}$	1, 2	Non-inverting and Inverting serial data inputs.	—	CML input
SDO/$\overline{SDO}$	12, 11	Non-inverting and inverting serial data outputs to coaxial cable.	—	CML output

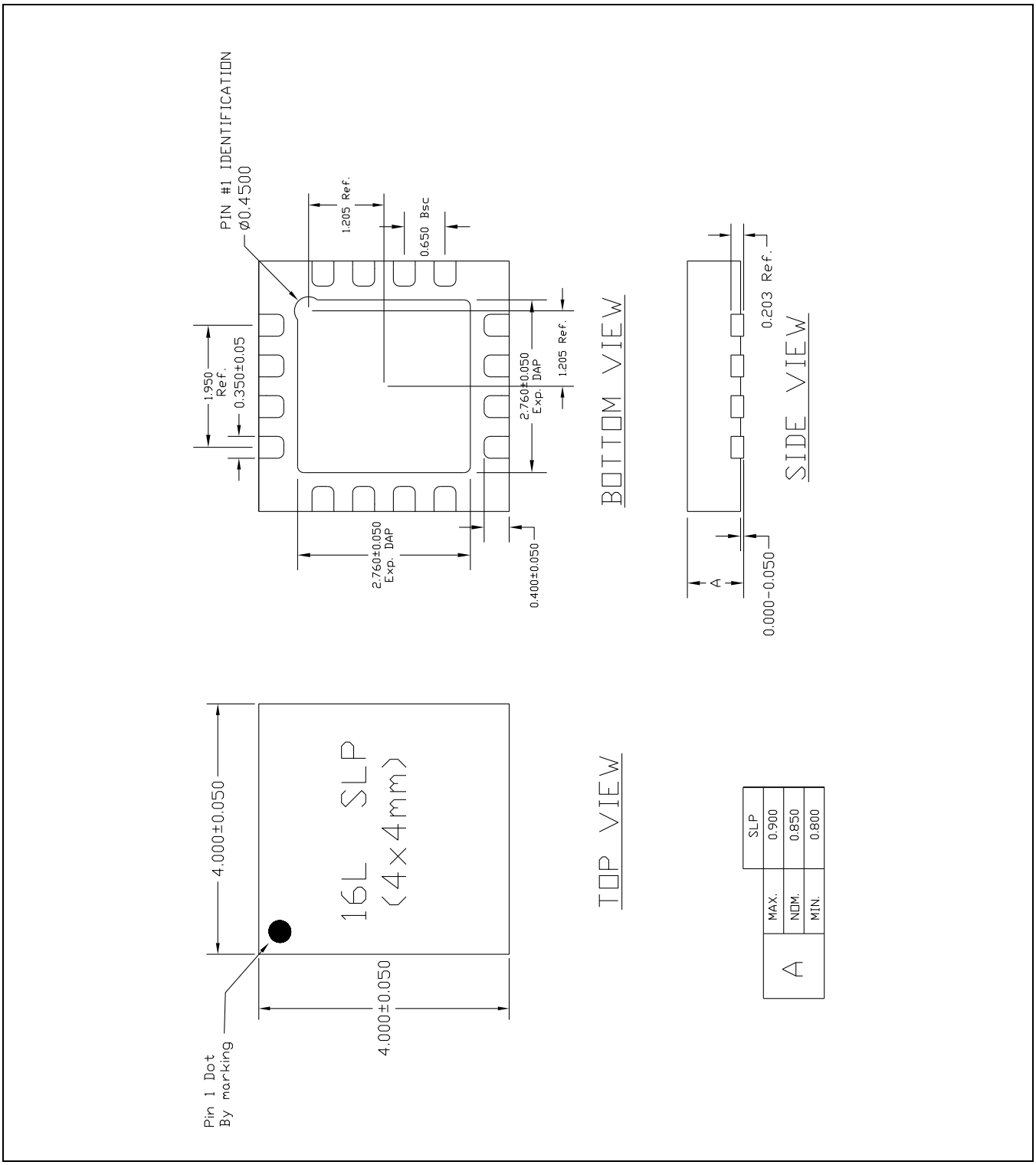
Table 2-5. Control Pins

Pin Name	Pin #	Function	Default	Type
SD/$\overline{\text{HD}}$	10	Input control signal to change the output slew rate. SD/$\overline{\text{HD}}$ = High: Slow output slew rate for SD SDI rate. SD/$\overline{\text{HD}}$ = Low: Fast output slew rate for HD and 3G SDI rate.	Pull-up	CMOS input
$\overline{\text{DISABLE}}$	6	A low disables the SDO/$\overline{\text{SDO}}$ outputs. A high enables the SDO/$\overline{\text{SDO}}$ outputs.	Pull-up	CMOS input
NOTES: Internal pull-ups/pull-downs are 100 kΩ.				

2.2 Packaging

The package for the M08028/M08038 is illustrated in Figure 2-2 below.

Figure 2-2. Package Drawing (4x4 mm, 16-pin QFN)



2.3 Manufactureability

The values shown in this section may change; however, these are standard requirements.

2.3.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000 V of ESD Human Body Model (HBM) testing.

Tested per JESD22-C101. This device passes 500 V of ESD Charged Device Model (CDM) testing.

Tested per EIA/JESD78. This device passes 150 mA of trigger current at 85 °C during Latchup testing.

2.3.2 Peak Reflow Temperature

M08028G/M08038G (RoHS compliant package): Peak reflow temperature is 260 °C per JEDEC standards.

3.0 Functional Description

3.1 Features

3.1.1 HD-SDI and SD-SDI Slew-rate Selection

The M08028/M08038 output slew rate is selectable. The slew rate will vary depending on the output matching network and connector used.

For HD and 3G data rates, with **SD/x$\overline{\text{HD}}$** = Low, rise/fall time is typically 100 ps. For SD data rates, with **SD/x$\overline{\text{HD}}$** = High, rise/fall time is typically 600 ps.

3.1.2 Output Amplitude Adjustment

A resistor connected to **RSET** pin is used to set the amplitude of the single-ended output swing.

An external 750 Ω ±1% resistor at **RSET** to **AV_{DD}** is recommended for an output swing of 800 mVpp within a tolerance that is less than ±10%. The output amplitude can also be adjusted to range from 500 to 1600 mVpp single-ended using the following formula:

Output Swing = (600/**RSET**) [**RSET** in kΩ] (in mVpp, single-ended)

The actual swing is set as a function of the IC supply voltage, the external termination voltage and the limitations are shown in Table 3-1. In applications where lossy matching or splitting networks are used, the M08028/M08038 offer additional gain of up to 1600 mVpp swing.

Table 3-1. Output Swing vs. Supply and Termination Voltage

AV_{DD} (V)	AV_{DDTERM} (V)	Maximum Swing (Single-ended mVpp)	Minimum Swing (Single-ended mVpp)
3.3	3.3	1200	500
3.3	5.0	1600	500

3.2 Pin Definitions

3.2.1 High-speed Inputs

The M08028/M08038 are designed to be operated with input signals as low as 100 mV_{PPD} or up to 2000 mV_{PPD}. The M08028/M08038 use external 50 Ω input termination resistors to match 100 Ω differential impedance transmission lines for improved system level performance. The M08028/M08038 recommended input circuits are shown in Figure 3-1 and Figure 3-2.

Figure 3-1. Typical Input Circuit—AC Coupled

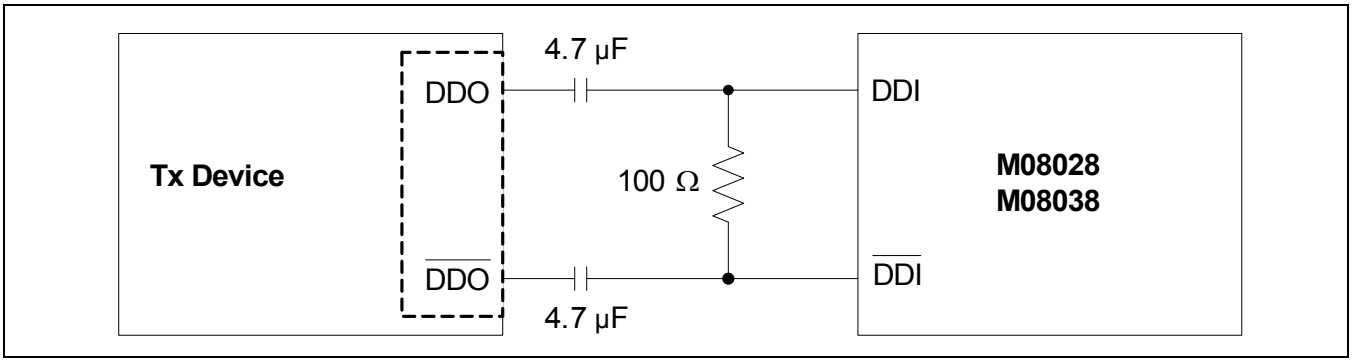
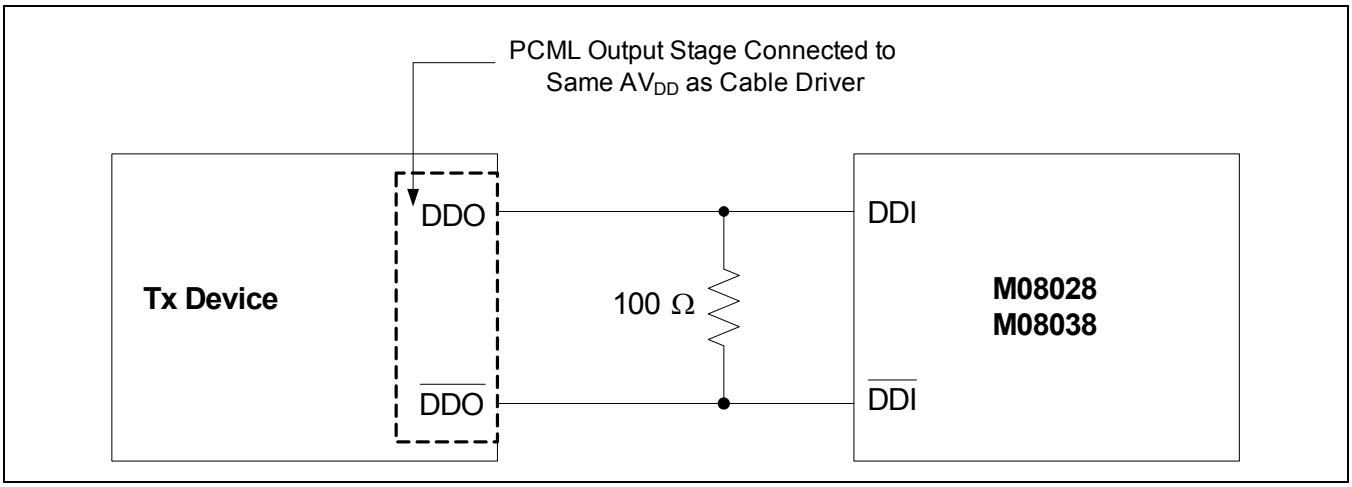


Figure 3-2. Typical Input Circuit—DC Coupled

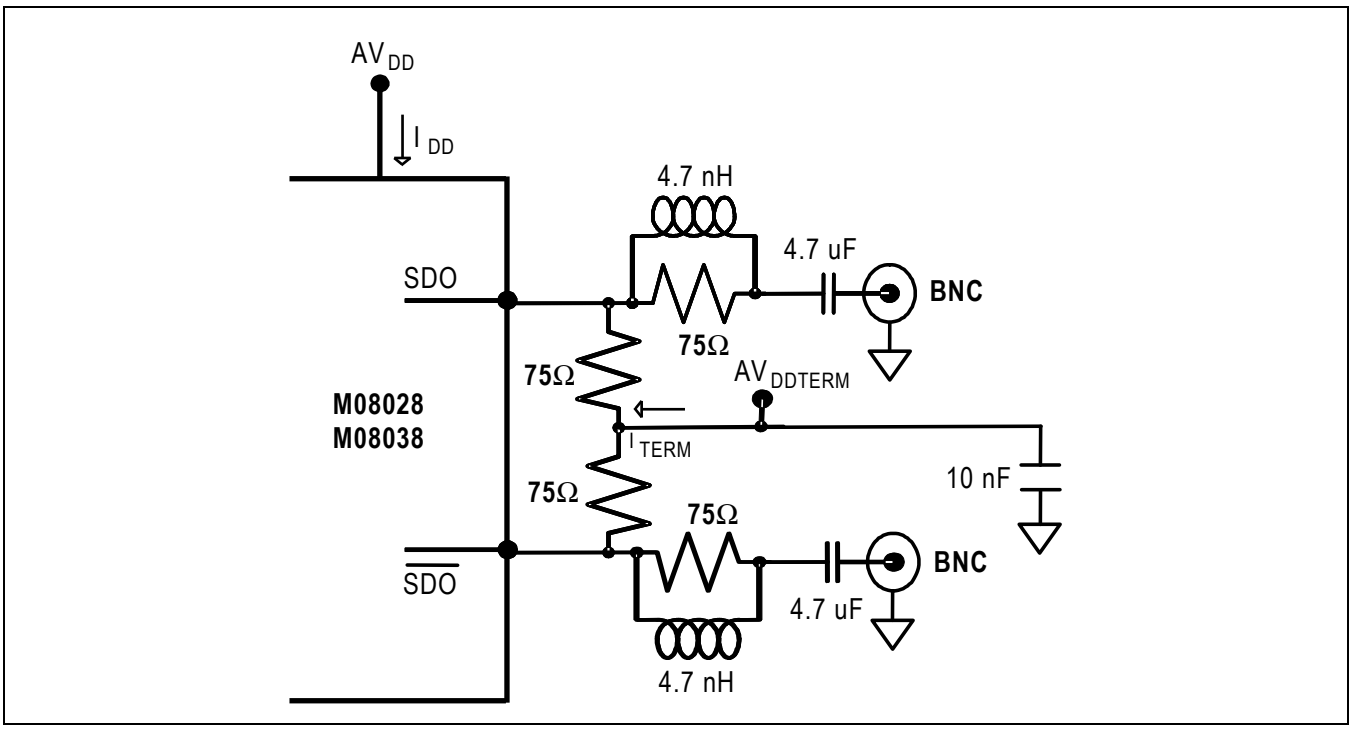


3.2.2 High-speed Outputs

The M08028/M08038 output buffer is an open collector buffer that is designed for a return loss of 15 dB at SD and HD rates and 10 dB at 3G rates, using standard through-hole BNC connectors. A typical output matching circuit is shown in Figure 3-3. The Output Return Loss (ORL) is dependent on many factors such as the value and type of components used, PCB layout, PCB trace lengths, and type of PCB di-electric, therefore, the recommendations in the figure below should be used as starting guidelines only. Different output matching network topologies and different component values will result in different ORL performance.

The actual maximum output of the part depends on the applied IC voltage as well as the external termination voltage for the load termination. The limitations are discussed in Section 3.1.

Figure 3-3. Typical Output Matching/Back-termination Circuit



Appendix

A.1 Glossary of Terms/Acronyms

BER	Bit Error Rate
CD	Cable Driver
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
EMI	Electro Magnetic Interference
EQ	Equalizer or Equalization
GREEN	Environmentally friendly
HD	High Definition
HW	Hardware
IC	Integrated Circuit
ID	Identifier
I/O	Input/Output
PCB	Printed Circuit Board
ORL	Output Return Loss
RoHS	Restriction of Hazardous Substances
SD	Standard Definition
SDI	Serial Digital Input
SDO	Serial Digital Output
SE	Single Ended
QFN	Quad Flat No-Lead

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- Application Notes for Surface Mount Assembly of Amkor's Packages
- Amkor Technology Thermal Test Report TT-00-06 (See http://www.amkor.com for detailed information)

www.mindspeed.com

General Information:
Telephone: (949) 579-3000
Headquarters - Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA 92660