M08026/M08036 SD, HD, 3G Cable Equalizer

The M08026/M08036 are high-speed, low-power, adaptive co-axial cable equalizers designed to increase the maximum low-jitter transmission distance of serial digital video signals across commonly used bandwidth-limiting 75 Ω coaxial cable. These devices automatically optimize the transfer function based on the bit rate and cable length to minimize the inter-symbol interference (ISI) jitter caused by the cable and to remove the DC offset components introduced with the pathological test pattern and AC coupling in systems.

The M08036 is designed to support SD, HD, and 3G data rates from 143 Mbps to 2970 Mbps. The M08026 is designed to support SD and HD data rates from 143 Mbps to 1485 Mbps.

The low-noise, high-gain equalizer allows for low jitter 3G transmissions up to 100 m (Belden 1694A) and HD transmissions up to a length of 200 m (Belden 1694A) and 120 m (Belden 8281). For SD data rates, cable lengths up to 400 m (Belden 1694A) and 300 m (Belden 8281) are supported.

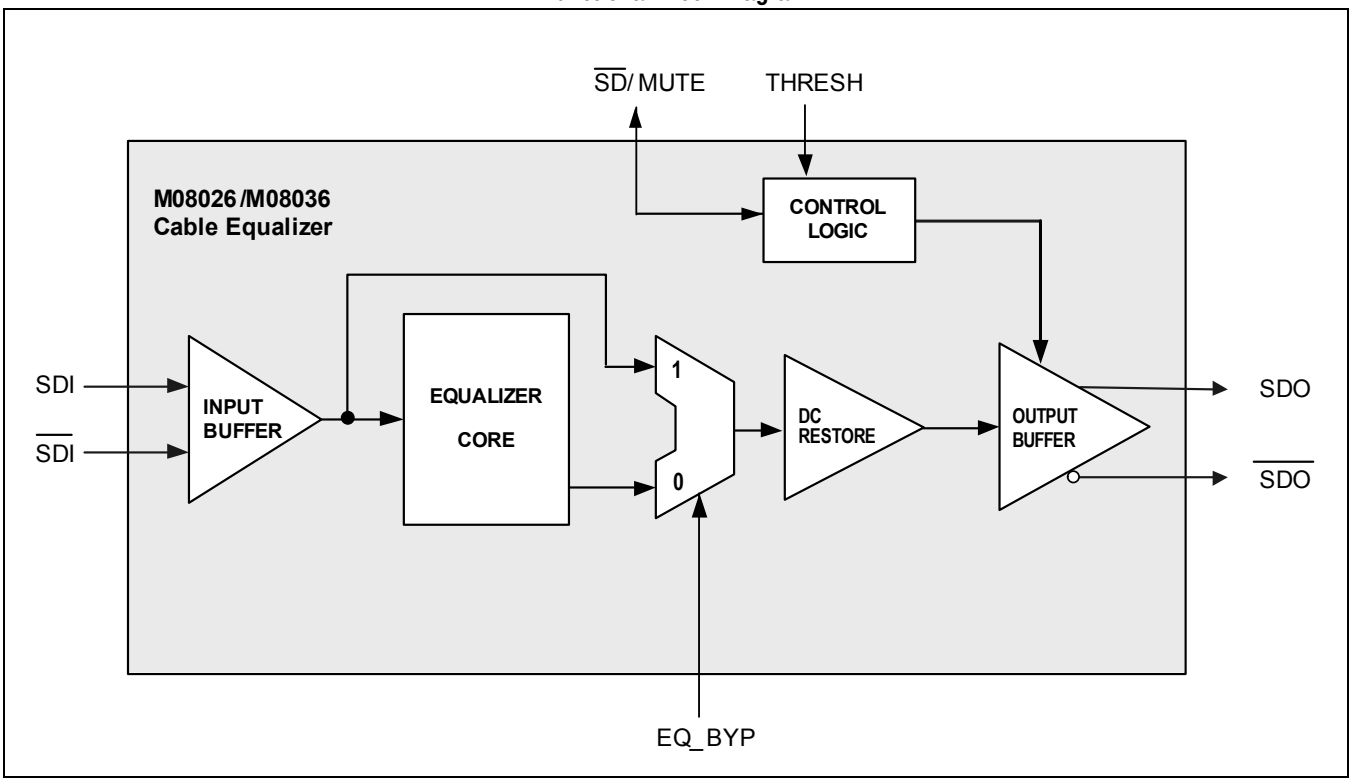
Features

- Adaptive cable equalization
- 3G, HD, and SD operation (M08036)
- HD and SD operation (M08026)
- Typical equalized length of Belden 1694A cable: 100 m at 2.97 Gbps, 200 m at 1.485 Gbps, and 400 m at 270 Mbps
- Programmable mute level
- Manual bypass mode
- Differential CML outputs (50 Ω on-chip terminations)
- Single 3.3 V power supply
- Small form factor (4x4 mm, 16-pin QFN package)
- Pb-free and RoHS compliant

Applications

- Digital Video Recorders (DVR)
- Video Mixers and Switchers
- Surveillance / CCTV Cameras
- Industrial and Professional Cameras
- Digital Image Capture Devices
- Digital Video Displays
- Distribution Amplifiers
- Repeaters

Functional Block Diagram



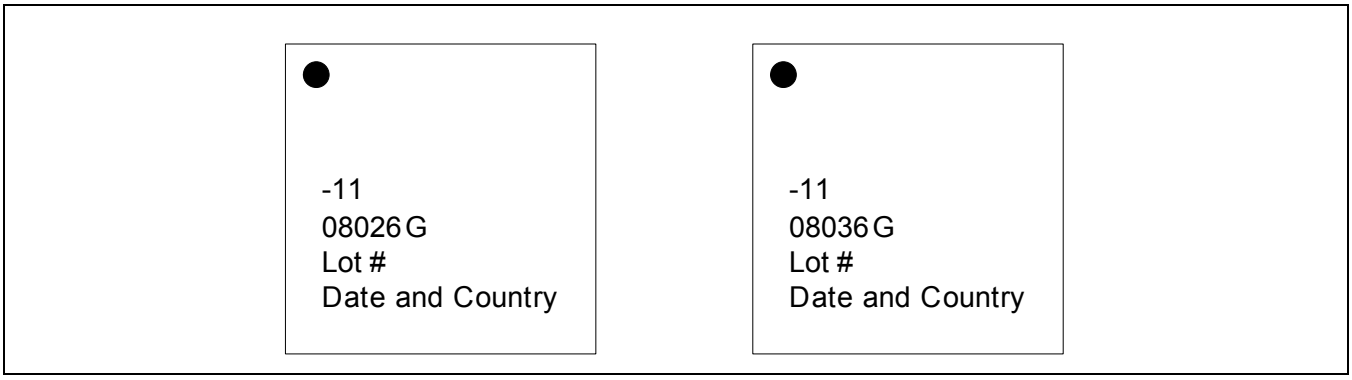
Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M08026G-11*	4x4 mm, 16-pin QFN (RoHS compliant)	143–1485 Mbps	–10 °C to 85 °C
M08036G-11*	4x4 mm, 16-pin QFN (RoHS compliant)	143–2790 Mbps	–10 °C to 85 °C
* The letter 'G' designator after the part number indicates a RoHS-compliant package. Refer to www.mindspeed.com for additional information.			

Revision History

Revision	Level	Date	Description
A	Release	May 2011	Released.

M08026/M08036 Marking Diagram



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
AV_{DD}	Positive Supply	AV_{SS} – 0.5	AV_{SS} + 3.6	V
$V_{MAX, IO}$	Maximum/minimum input/output voltage on any input/output pin	AV_{SS} – 0.5	AV_{DD} + 0.5	V
T_{STORE}	Storage Temperature	–65	+150	°C
$V_{ESD, HBM}$	Human Body Model	2000	—	V
$V_{ESD, CDM}$	Charge Device Model	500	—	V

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	Supply Voltage	—	3.13	3.3	3.46	V
T_{AMB}	Ambient Temperature	—	–10	—	+85	°C
θ_{JA}	Junction to Ambient Thermal Resistance	1, 2	—	44.5	—	°C/W

NOTES:

1. Mounted on multi layer board (≥ 4 layers).
2. Airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Typical	Maximum	Units
I_{DD}	Supply Current	1	70	90	mA
P_{TOTAL}	Total Power Dissipation (AV_{DD} = 3.3 V)	1, 2, 3	230	312	mW

NOTES:

1. Specified at recommended operating conditions in Table 1-2.
2. Includes on-chip power dissipation as well as off-chip power dissipated by termination resistors.
3. Typical calculated at nominal supply voltage, maximum calculated at nominal supply voltage + 5%.

Table 1-4. CMOS Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic high)	1	–100	100	µA
I_{IL}	Input Current (logic low)	1	–100	100	µA

NOTE:

1. Specified at recommended operating conditions in Table 1-2. Spec is for a max load of 20 pF.

Table 1-5. High-Speed Input Electrical Specifications (M08026)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input Bit Rate	1	143	—	1485	Mbps
V_{IN}	Differential Input Swing	1, 5	700	800	1200	mV_{PPD}
V_{ICM}	Input Common-Mode Voltage	1, 4	—	2.75	—	V
C_{IN}	Input capacitance	1, 4	—	0.5	—	pF
R_{IN}	Input resistance	1, 4	—	1.6	—	kΩ
S_{11}	Input Return Loss (5 MHz to 1.5 GHz)	1, 2, 3	20	30	—	dB

NOTES:

1. Specified at recommended operating conditions in Table 1-2.
2. Using the recommended input termination shown in Figure 3-1.
3. Measured single ended.
4. Guaranteed by design.
5. 0 m of cable. This is also the recommended cable launch level (far end).

Table 1-6. High-Speed Input Electrical Specifications (M08036)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input Bit Rate	1	143	—	2970	Mbps
V_{IN}	Differential Input Swing	1, 5	700	800	1200	mV_{PPD}
V_{ICM}	Input Common-Mode Voltage	1, 4	—	2.75	—	V
C_{IN}	Input capacitance	1, 4	—	0.5	—	pF
R_{IN}	Input resistance	1, 4	—	1.6	—	kΩ
S_{11}	Input Return Loss (5 MHz to 1.5 GHz)	1, 2, 3	20	30	—	dB
S_{11}	Input Return Loss (1.5 GHz to 3 GHz)	1, 2, 3	3	—	13	dB

NOTES:

1. Specified at recommended operating conditions in Table 1-2.
2. Using the recommended input termination shown in Figure 3-1.
3. Measured single ended.
4. Guaranteed by design.
5. 0 m of cable. This is also the recommended cable launch level (far end).

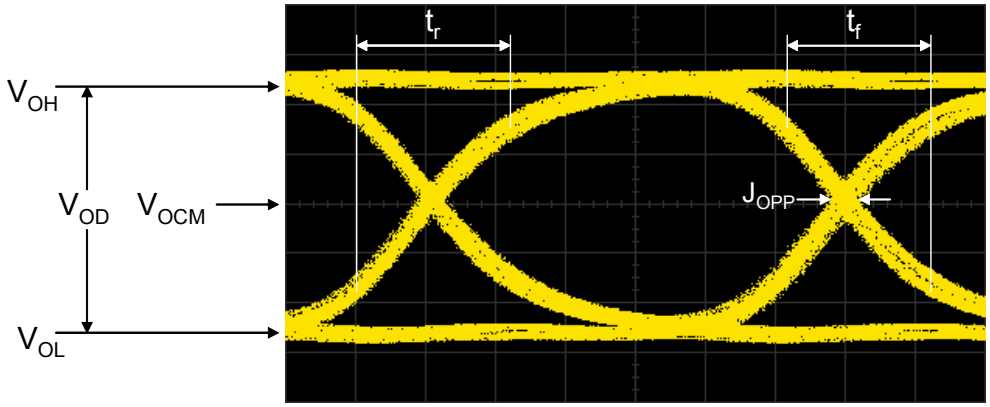
Table 1-7. High-Speed Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_R/t_F	Rise/Fall Time (20%–80%)	1, 2, 7	—	100	120	ps
$t_R/t_F \Delta$	Mismatch between output rise/fall times	1, 2, 7	—	0	30	ps
DCD_{DATA}	Duty Cycle Distortion (DCD)	1, 2, 5, 6	—	0	15	ps
V_{OUT}	Differential Output Swing	1, 3	600	750	950	mV_{PPD}
V_{OCM}	Common mode Voltage	1, 3, 4	—	AV_{DD} – 0.205	—	V
R_{OUT}	Internal Output Termination Resistance to AV_{DD}	1	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions in Table 1-2.
2. With 100 Ω differential termination.
3. With 50 Ω to AV_{DD} termination.
4. Outputs DC-coupled.
5. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
6. Measured with a 1010 pattern.
7. Measured with a PRBS23 pattern.

Figure 1-1. Output Symbols Definition



V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

Table 1-8. Cable Equalizer Distance Specifications

Symbol	Parameter	Conditions	Notes	Maximum	Units
L_{SD}	Cable Length	Belden 1694A	1, 4	400	m
	Cable Length	Belden 8281	1, 4	300	m
L_{HD}	Cable Length	Belden 1694A	2, 6	200	m
	Cable Length	Belden1694A	2, 5	140	m
	Cable Length	Belden 8281	2, 5	120	m
L_{3G}	Cable Length	Belden 1694A	3, 6	100	m

NOTES:

Entire table specified at recommended operating conditions in Table 1-2.

1. Data Rate = 270 Mbps.
2. Data Rate = 1485 Mbps.
3. Data Rate = 2970 Mbps.
4. Error Free with timing jitter typically = 0.2 UI, pathological pattern.
5. Error Free with alignment jitter typically = 0.25 UI, pathological pattern.
6. Error Free with alignment jitter typically = 0.3 UI, pathological pattern.

Table 1-9. LOS/MUTE Output Voltage Specifications

Symbol	Parameter	Notes	Typical	Units
$V_{LOS, OL}$	LOS/Mute pin output voltage when input signal detected	1	0.16 x AV_{DD}	V
$V_{LOS, OH}$	LOS/Mute pin output voltage when input signal not detected	1	0.95 x AV_{DD}	V

NOTE:

1. Specified at recommended operating condition in Table 1-2.

Please see Amkor's Application Note for PCB footprint (referenced in the Section A.2.1).

2.0 Pinout Diagram, Pin Descriptions, and Package Outline Diagram

The pin assignment is illustrated in Figure 2-1. The M08026/M08036 packages are RoHS compliant. These packages are backwards compatible with the standard soldering techniques as defined in JEDEC-STD-020C (SnPb Process).

Figure 2-1. M08026/M08036 Pinout Diagram

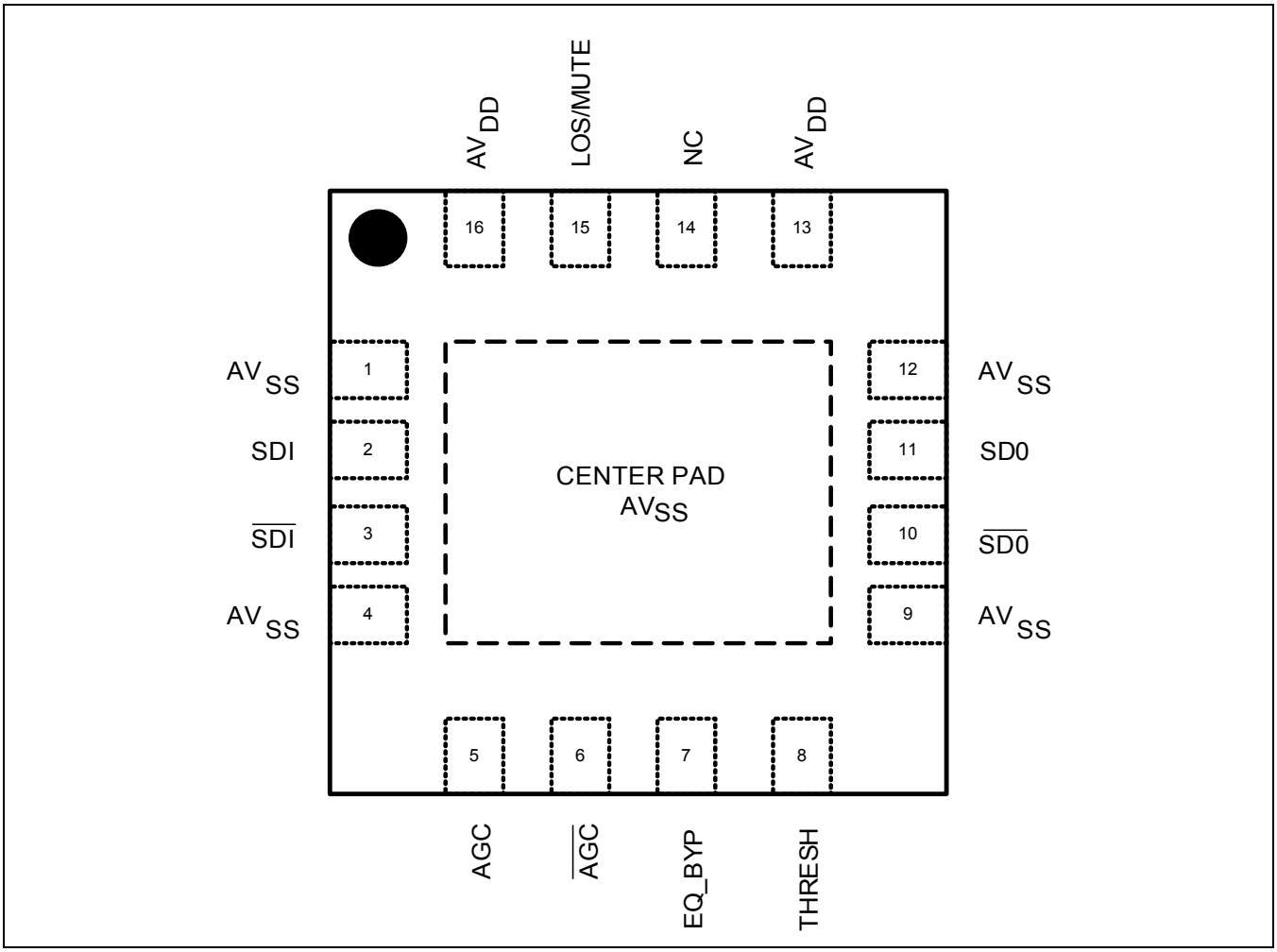


Table 2-1. M08026/M08036 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	13, 16	Power	Analog positive supply
AV_{SS}	1, 4, 9, 12	Power	Ground
SDI/$\overline{SDI}$	2, 3	CML input	High-speed serial digital input
SDO/$\overline{SDO}$	11, 10	CML output	High-speed serial digital output
AGC/$\overline{AGC}$	5, 6	Analog input	Internal pull up
EQ_BYP	7	CMOS input	Internal pull down
THRESH	8	Analog input	Internal pull down
LOS/MUTE	15	CMOS input/output	Bi-directional signal Input control signal or output
NC	14	N/A	Do not connect

2.1 M08026/M08036 Signals by Interface Group

Table 2-2. Power Pins

Pin Name	Pin Number	Function	Type
AV_{SS}	1, 4, 9, 12	Ground	Power
AV_{DD}	13, 16	Positive Supply	Power
Center Pad	—	Chip Ground	Power

Table 2-3. High-speed Signal Pins

Pin Name	Pin Number	Function	Type
SDI/$\overline{SDI}$	2, 3	Non-inverting and Inverting Serial Data Input to the adaptive equalizer	CML input
SDO/$\overline{SDO}$	11, 10	Non-inverting and Inverting Differential Serial Data Output	CML output

Table 2-4. Control/Interface Pins

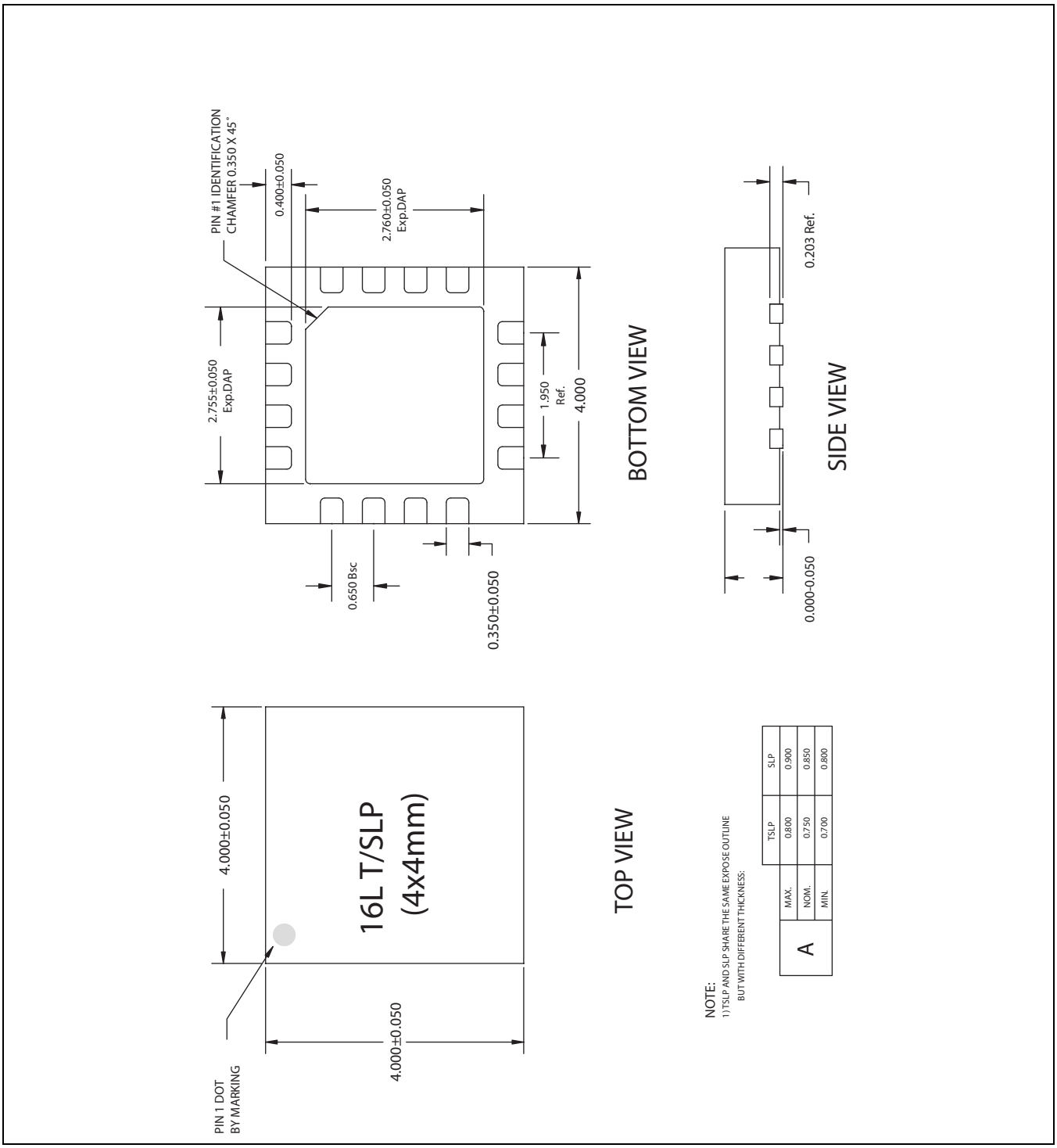
Pin Name	Pin Number	Function	Default	Type
AGC/$\overline{\text{AGC}}$	5, 6	External AGC (Automatic Gain Control) capacitor connection points. Use 1.0 µF capacitor.	Internal pull up	Analog input
EQ_BYP	7	Input control signal that when enabled (High) bypasses the inputs directly to the output stage. Low = Normal operation High = Disables EQ and bypasses input to output	Internal pull down	CMOS input
NC	14	Do not connect.	N/A	N/A
THRESH	8	Input control signal voltage. Programmable cable length forced mute threshold. This function is disabled if **LOS/MUTE** = Low	Internal pull down	Analog input
LOS/MUTE	15	Bidirectional signal that can be used as an input control signal or as an output status indicator. When configured as an input by forcing a voltage on **LOS/MUTE** = High, the SDO outputs will be inhibited at logic low (outputs muted). See Table 1-4 for CMOS input levels. When **LOS/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled. When configured as an output (tied to a high-impedance input) or left floating, the programmable inhibit based on cable length is enabled. See Table 1-9 for LOS/MUTE pin output levels. Configured as Output: Low = Input signal detect High = Loss of signal Configured as Input: Low = Never mute High = Force Mute	—	CMOS input/ output

NOTE:
Internal pull-up/pull-down is 100 kΩ.

2.1.1 Packaging

The package for the M08026/M08036 is illustrated in Figure 2-2 below.

Figure 2-2. M08026/M08036 Package Outline Drawing



Please see Amkor's Application Note for PCB footprint (referenced in the Section A.2.1).

2.2 Manufactureability

The values shown in this section may change; however, these are standard requirements.

2.2.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000 V of ESD Human Body Model (HBM) testing.
Tested per JESD22-C101. This device passes 500 V of ESD Charged Device Model (CDM) testing.
Tested per EIA/JESD78. This device passes 150 mA of trigger current at 85 °C during Latchup testing.

2.2.2 Peak Reflow Temperature

M08026/M08036 (RoHS compliant package): Peak reflow temperature is 260 °C per JEDEC standards.

2.2.3 Moisture Sensitivity Level (MSL)

All versions of this device (Std Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

3.0 Functional Description

3.1 General Nomenclature

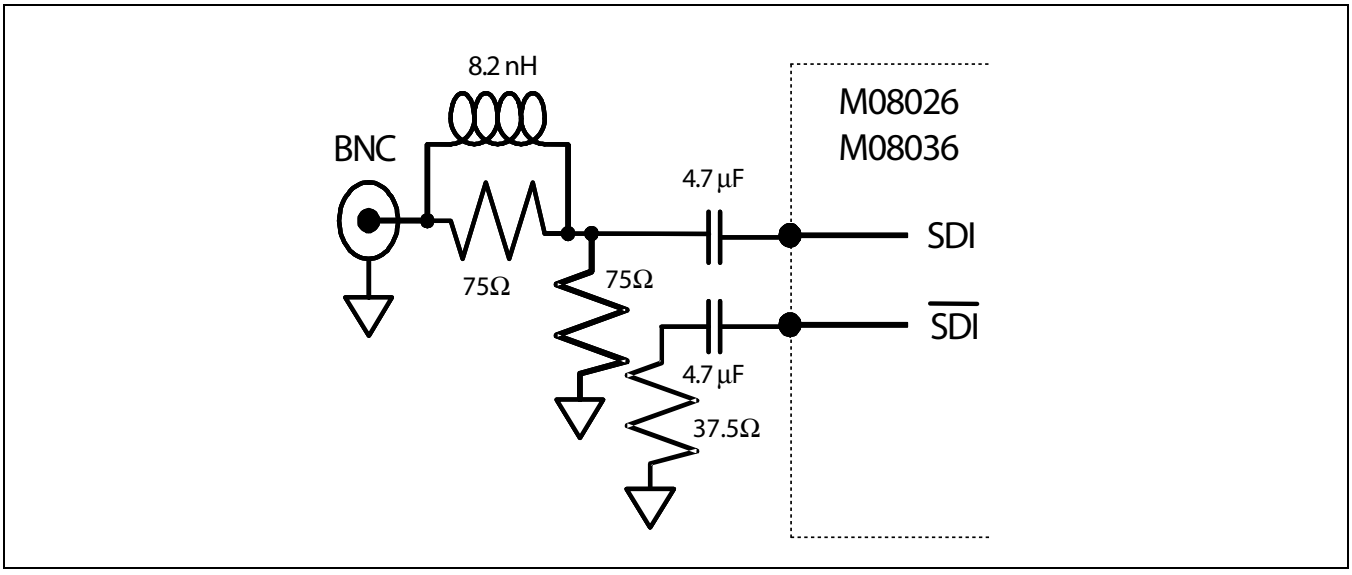
Throughout this data sheet, physical pins will be denoted in **BOLD** print.

3.2 High-Speed Input

Digital video coaxial cables are AC-coupled to the high-speed low-noise inputs, **SDI/$\overline{\text{SDI}}$**, which, are designed to operate in both the single-ended or differential mode. The typical application is single-ended into the non-inverting **SDI** input with the inverting **$\overline{\text{SDI}}$** input biased to match the bias on the input used.

The M08026/M08036 do not contain any internal input terminations and require external input termination as well as matching circuit to improve input return loss. The package and IC design of the M08026/M08036 have been optimized for high-speed performance, allowing it to have typical return loss values of 13 dB at 3 GHz and 30 dB at 1.485 GHz, using the recommended external matching/termination network and commonly employed right-angle, through-hole, or vertical mount 75 Ω BNC connectors. For non-inverting single-ended operation, the recommended input circuit is shown in Figure 3-1. For differential operation, the matching/termination circuit on **SDI** should be duplicated on **$\overline{\text{SDI}}$**. The internal pull ups automatically bias **SDI/$\overline{\text{SDI}}$** for proper AC coupled operation.

Figure 3-1. Single-ended Typical Input Matching/Termination Network



3.3 High-Speed Outputs

The high-speed differential outputs after equalization are made available on the **SDO/xSDO** pins.

3.4 Adaptive Equalization Selection

In typical operation, the adaptive equalization is enabled with **EQ_BYP** = Low; however, with **EQ_BYP** = High, the adaptive equalization and DC restore circuit is bypassed and the input is fed directly to the output.

3.5 Output Mute and Loss of Signal Detect

LOS/MUTE is a bi-directional pin that acts as an LOS detect output or a MUTE input.

When a voltage is forced on the pin, **LOS/MUTE** is a MUTE input. With **LOS/MUTE** = High (V_{DD}), the outputs of the M08026/M08036 will be inhibited at logic low. When **LOS/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled.

When the pin is tied to a high impedance node or left floating, **LOS/MUTE** is an LOS indicator output. In the event of an LOS, the output is muted. The inhibit threshold is set with an analog voltage applied to the THRESH input pin. This threshold will depend on cable type (e.g. Belden 1694A or 8281). To achieve maximum cable length equalization, the THRESH pin should be left open. Decoupling capacitors should be used between the THRESH pin and GND.

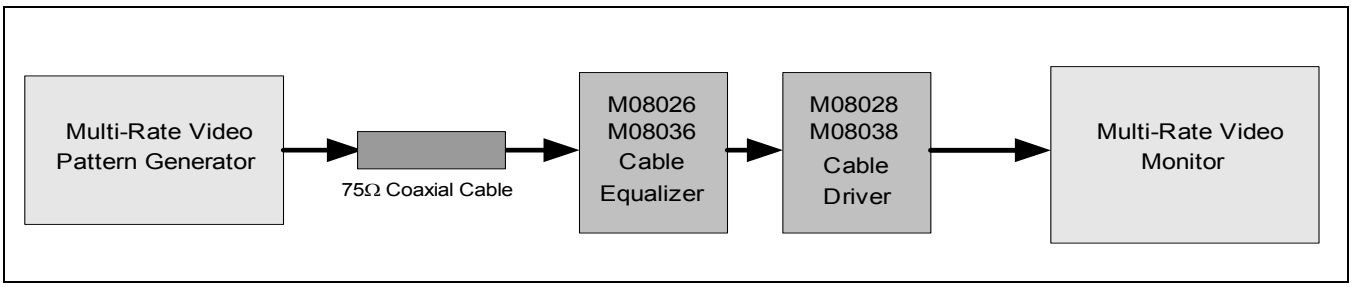
3.6 Equalizer Detailed Description

The basic equalizer design consists of interlaced stages of gain and equalization to maximize both the overall equalization gain as well as the input sensitivity for maximum performance with minimum jitter. In order to achieve maximum distance at 270 Mbps, 1485 Mbps, and 2970 Mbps with Belden 1694A, the overall equalizer block has over 50 dB of broadband signal boost and maintains an input sensitivity of approximately 10 mV. Using a high-performance silicon process, high gain-bandwidth products are achieved allowing for high-performance, wide dynamic range design with minimum power dissipation.

Since signals are launched with different rise and fall times which can vary substantially (especially at the receive end after going though a wide dynamic range of valid cable lengths) the equalization routine determines both the bit rate and the resultant signal HF attenuation as opposed to just looking at the launch edge rates. By determining both sets of conditions, it is possible to optimize the equalizer for the different rates. For example, the M08026/M08036 maintain the same maximum cable length as optimized SD only equalizers. An SD signal through a short cable can have the same edge rate as a HD signal through a long cable; yet, both conditions require different levels of equalization as well as different optimized inverse-transfer functions. The advanced equalization technology can make the distinction between the two cases for optimal performance. This also leads to proper mute threshold (**THRESH**) that is independent of the bit rate.

In order to accommodate both the worst case equalizer pathological patterns as well as some customer derived worst case DC offset patterns, a high-gain slicer is included in the signal path to correct for any eye-crossing wander due to AC coupling of the input. Figure 3-2 shows the test setup used by Mindspeed to evaluate the performance of the M08026/M08036.

Figure 3-2. Test Setup Diagram for Cable Equalizer Evaluation



Appendix

A.1 Glossary of Terms/Acronyms

BER	Bit Error Rate
CD	Cable Driver
CML	Current Mode Logic
DDI	Differential Data Inputs
EMI	Electro Magnetic Interference
EQ	Equalizer or Equalization
ESD	Electro Static Discharge
GREEN	Environmentally friendly
HD	High Definition
HW	Hardware
ID	Identifier
I/O	Input/Output
QFN	Quad Flat No Lead
RoHS	Restriction of Hazardous Substances
SD	Standard Definition
SDI	Serial Digital Input
SDO	Serial Digital Output
SE	Single Ended
SW	Software

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- Application Notes for Surface Mount Assembly of Amkor's Quad Flat No Lead (QFN) Packages
- Amkor Technology Thermal Test Report TT-00-06 (See http://www.amkor.com for detailed information)

www.mindspeed.com

General Information:
Telephone: (949) 579-3000
Headquarters - Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA 92660