M08046

SD, HD, and 3G Cable Equalizer

The M08046 is a high-speed, low-power, adaptive co-axial cable equalizer designed to increase the maximum low-jitter transmission distance of serial digital interface (SDI) video signals across commonly used bandwidth-limiting 75 Ω coaxial cable. This device automatically optimizes its transfer function based on the bit rate and cable length to minimize the inter-symbol interference (ISI) jitter caused by the cable and to remove the DC offset components introduced with the pathological test pattern and AC coupling in systems.

The M08046 is designed to support SD, HD, and 3G data rates from 143 Mbps to 2970 Mbps.

The low-noise, high-gain equalizer allows for low jitter 3G-SDI transmissions up to 100 m (Belden 1694A) and HD transmissions up to a length of 200 m (Belden 1694A) and 120 m (Belden 8281). For SD data rates, cable lengths up to 400 m (Belden 1694A) and 300 m (Belden 8281) are supported.

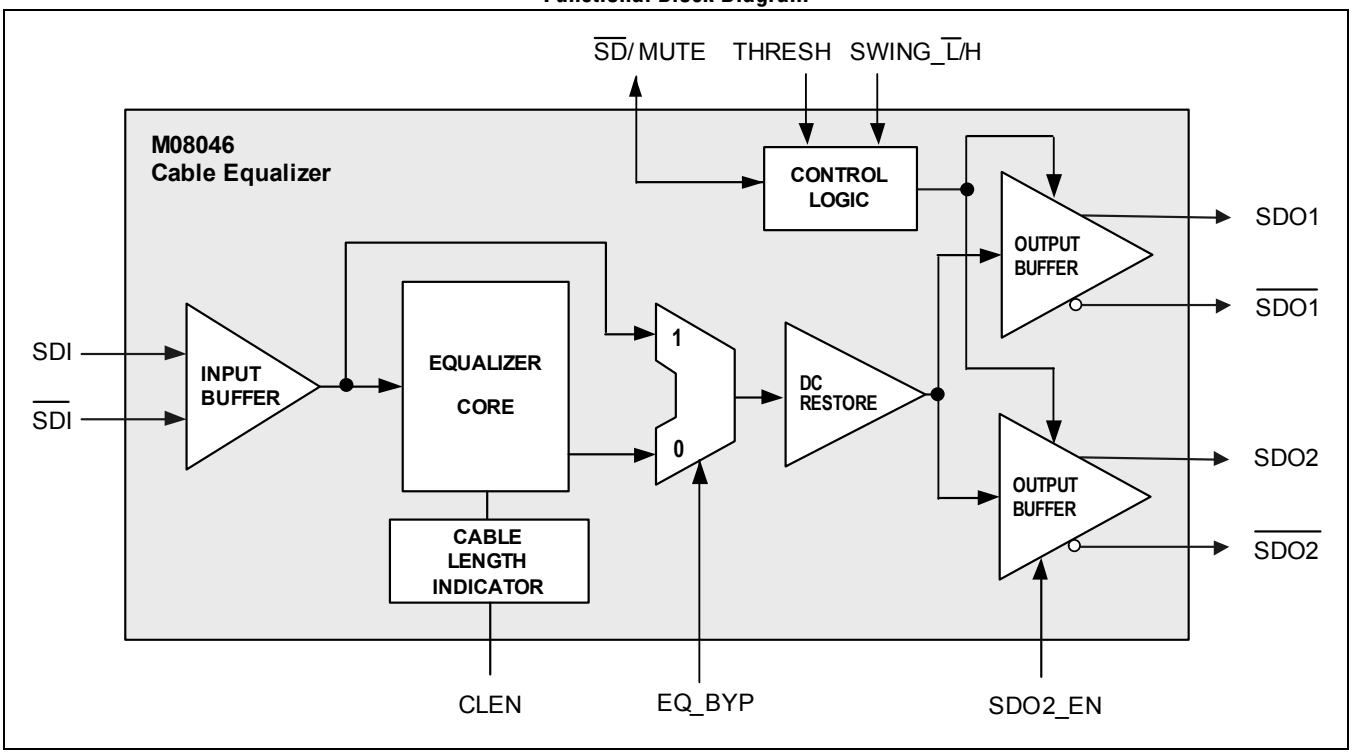
Applications

- Digital Video Recorders (DVR)
- Video Mixers and Switchers
- Surveillance / CCTV Cameras
- Industrial and Professional Cameras
- Digital Image Capture Devices
- Digital Video Displays
- Distribution Amplifiers
- Repeaters

Features

- Dual CML outputs, with selectable high amplitude
- Enable for second CML output
- 2.5 V or 3.3 V Supply
- Low Power (175 mW @ 2.5 V, 230 mW @ 3.3 V)
- Adaptive cable equalization
- 3G, HD, and SD operation
- Typical equalized length of Belden 1694A cable: 100 m at 2.97 Gbps, 200 m at 1.485 Gbps, and 400 m at 270 Mbps
- Programmable mute level
- Manual bypass mode
- Small form factor (5x5 mm, 32-pin QFN package)
- Pb-free and RoHS compliant

Functional Block Diagram



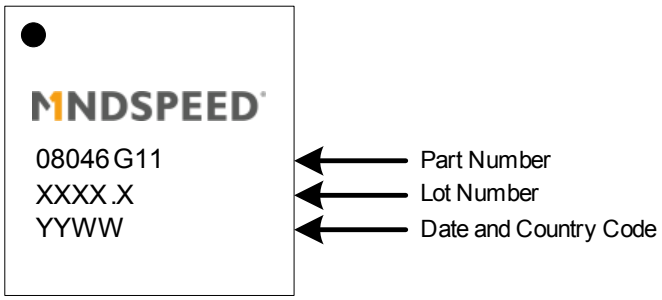
Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M08046G-11*	32-pin QFN (RoHS compliant)	143–2970 Mbps	–10 °C to 85 °C
* The letter 'G' designator after the part number indicates an RoHS-compliant package. Refer to www.mindspeed.com for additional information.			

Revision History

Revision	Level	Date	Description
A	Release	May 2011	Initial Release.

M08046 Marking Diagram



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1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
AV_{DD}	Positive Supply	AV_{SS} - 0.5	AV_{SS} + 3.6	V
$V_{MAX, IO}$	Maximum/minimum voltage on any input/output pin	AV_{SS} - 0.5	AV_{DD} + 0.5	V
T_{STORE}	Storage Temperature	–65	+150	°C
$V_{ESD, HBM}$	Human Body Model (low-speed)	2000	—	V
$V_{ESD, HBM}$	Human Body Model (high-speed)	2000	—	V
$V_{ESD, CDM}$	Charge Device Model	500	—	V

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	Supply Voltage	—	2.37	2.5/3.3	3.47	V
T_{AMB}	Ambient Temperature	—	–10	—	+85	°C
θ_{JA}	Junction to Ambient Thermal Resistance	1, 2	—	40	—	°C/W

NOTES:

1. Mounted on multi layer board (≥ 4 layers).
2. Airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Typical	Maximum	Units
I_{DD}	Supply Current	1	70	90	mA
P_{TOTAL}	Total Power Dissipation (@2.5 V)	1, 2, 3	175	236	mW
P_{TOTAL}	Total Power Dissipation (@3.3 V)	1, 2, 3	230	312	mW

NOTES:

1. Specified at recommended operating conditions — See Table 1-2.
2. Includes on-chip power dissipation as well as off-chip power dissipated by termination resistors.
3. Typical calculated at nominal supply voltage, maximum calculated at nominal supply voltage + 5%.

Table 1-4. CMOS Input Electrical Specifications (Logic Signals Only)

Symbol	Parameter	Notes	Minimum	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic high)	1	–100	100	µA
I_{IL}	Input Current (logic low)	1	–100	100	µA

NOTE:

1. Specified at recommended operating conditions — See Table 1-2. Spec is for a max load of 20 pF.

Table 1-5. High Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input Bit Rate	1	143	—	2970	Mbps
V_{IN}	Input Voltage Range with 0 m of cable, AV_{DD} = 2.5 or 3.3 V	1, 5	700	800	1200	mV_{PP}
$V_{CM, IN}$	Input Common-Mode Voltage (AV_{DD} = 3.3 V)	1, 4	—	2.75	—	V
	Input Common-Mode Voltage (AV_{DD} = 2.5 V)	1, 4	—	1.95	—	V
C_{IN}	Input capacitance	1, 4	—	0.5	—	pF
R_{IN}	Input resistance	1, 4	—	1.6	—	kΩ
S_{11}	Input Return Loss (5 MHz to 1.5 GHz)	1, 2, 3	20	30	—	dB
	Input Return Loss (1.5 GHz to 3 GHz)	1, 2, 3	—	13	—	dB

NOTES:

1. Specified at recommended operation conditions — See Table 1-2.
2. Using the recommended input termination shown in Figure 3-1.
3. Measured single ended.
4. Guaranteed by design.
5. This is also the recommended cable launch level (far end).

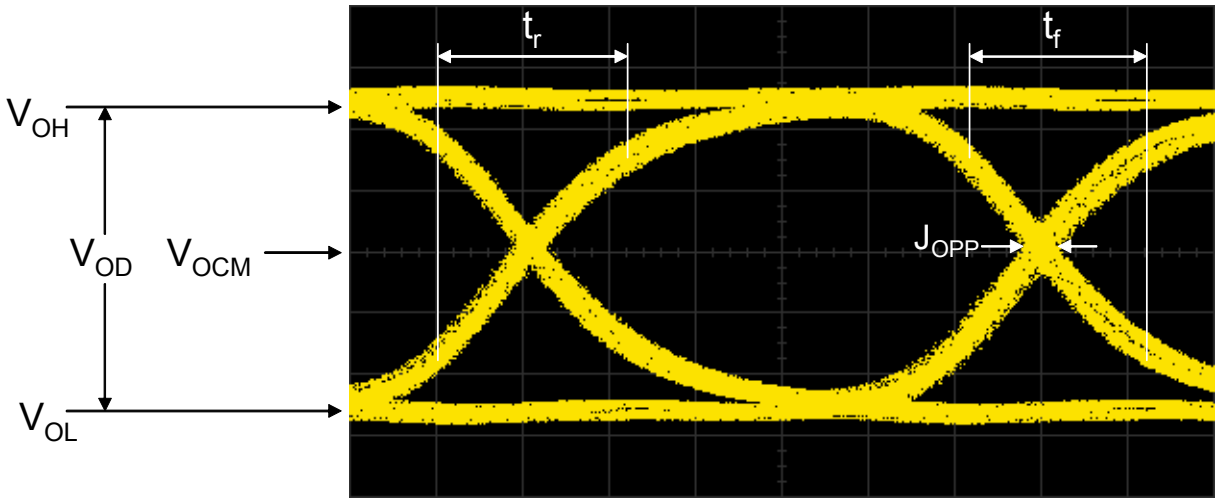
Table 1-6. High Speed Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_R/t_F	Rise/Fall Time (20%–80%)	1, 2, 7	—	100	120	ps
t_R/t_F Δ	Rise/Fall Time Mismatch	1, 2, 7	—	0	30	ps
DCD_{DATA}	Duty Cycle Distortion	1, 2, 5, 6	—	0	15	ps
V_{OD}	Differential Output Voltage HiSwEn = 0 (750 mV)	1, 3	600	750	950	mV_{PPD}
V_{OCM}	Common mode Voltage HiSwEn = 0 (750 mV)	1, 3, 4	—	AV_{DD} – 0.205	—	V
V_{OD}	Differential Output Voltage HiSwEn = 1 (1050 mV)	1, 3	850	1050	1270	mV_{PPD}
V_{OCM}	Common mode Voltage HiSwEn = 1 (1050 mV)	1, 3, 4	—	AV_{DD} – 0.290	—	V
R_{OUT}	Internal Output Termination Resistance to AV_{DD}	1	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions — See Table 1-2.
2. With 100 Ω differential termination.
3. With 50 Ω to AV_{DD} termination.
4. Outputs DC-coupled.
5. Duty Cycle Distortion is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then $DCD_{DATA} = 0$.
6. Measured with a 1010 pattern.
7. Measured with a PRBS23 pattern.

Figure 1-1. Output Symbols Definition



V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

Table 1-7. Cable Equalizer Distance Specifications

Symbol	Parameter	Conditions	Notes	Maximum	Units
L_{SD}	Cable Length	Belden 1694A	1, 4	400	m
	Cable Length	Belden 8281	1, 4	300	m
L_{HD}	Cable Length	Belden 1694A	2, 6	200	m
	Cable Length	Belden1694A	2, 5	140	m
	Cable Length	Belden 8281	2, 5	120	m
L_{3G}	Cable Length	Belden 1694A	3, 7	100	m

NOTES:

Entire table specified at recommended operating conditions — See Table 1-2.

1. Data Rate = 270 Mbps.
2. Data Rate = 1485 Mbps.
3. Data Rate = 2970 Mbps.
4. Error Free with timing Jitter typically = 0.2 UI, pathological pattern.
5. Error Free with alignment Jitter typically = 0.25 UI, pathological pattern.
6. Error Free with alignment jitter typically = 0.3 UI, pathological pattern.
7. Error Free with alignment Jitter typically = 0.35 UI, pathological pattern.

Table 1-8. xSD/MUTE Output Specifications

Symbol	Parameter	Notes	Typical	Units
$V_{LOS, OH}$	Output voltage when input signal detected	1	0.16 x AV_{DD}	V
$V_{LOS, OL}$	Output voltage when input signal not detected	1	0.95 x AV_{DD}	V

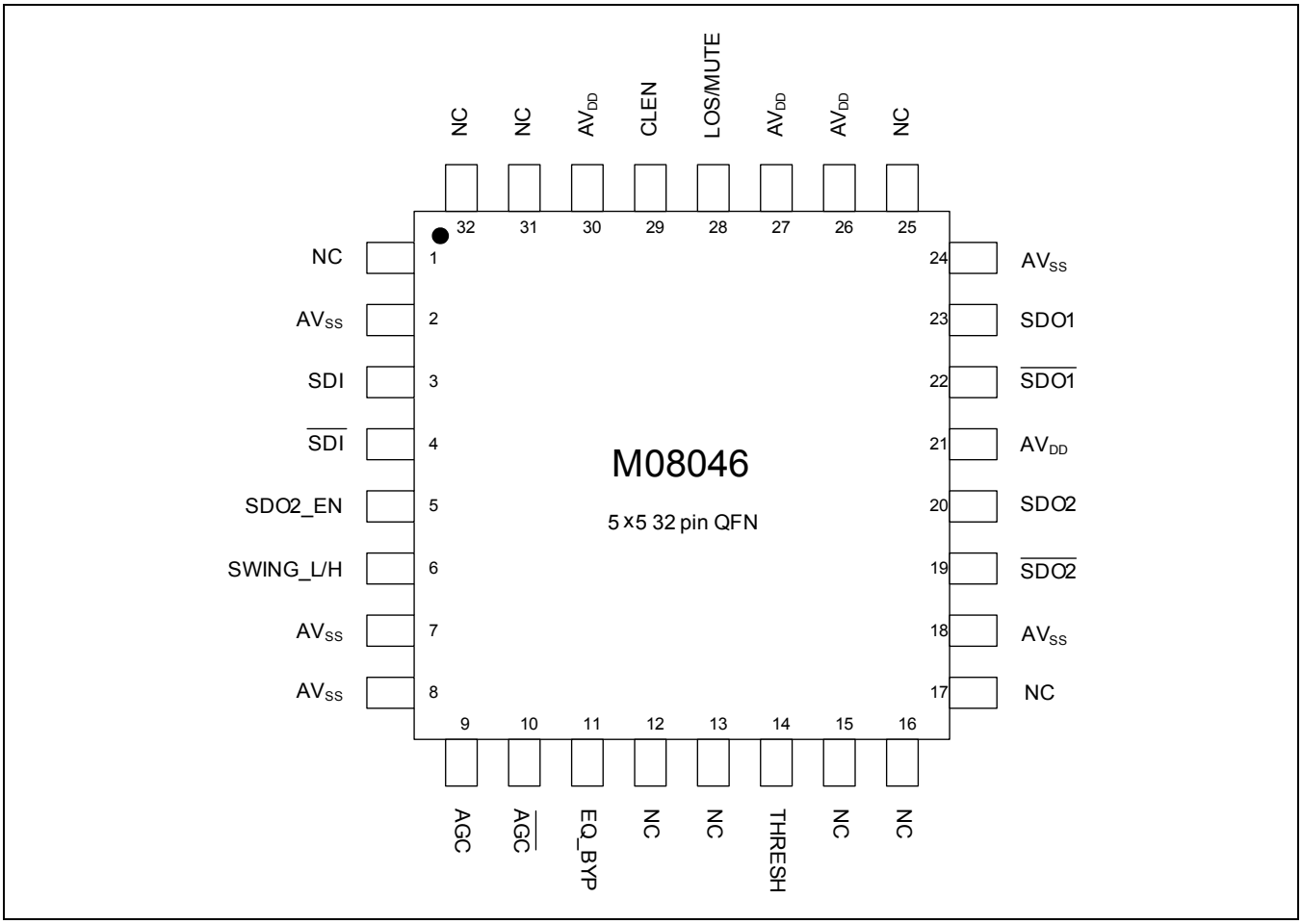
NOTE:

1. Specified at recommended operating condition — See Table 1-2.

2.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

The pin assignment is illustrated in Figure 2-1. The M08046 package is RoHS compliant. This package is backwards compatible with the standard soldering techniques as defined in JEDEC-STD-020C (SnPb Process).

Figure 2-1. M08046 Pin Assignments



2.1 Pin Descriptions

Table 2-1. Power Pins

Pin Name	Pin Number	Function	Type
AV_{SS}	2, 7, 8, 18, 24	Ground	Power
AV_{DD}	21, 26, 27, 30	Positive Supply	Power

Table 2-2. High-speed Signal Pins

Pin Name	Pin Number	Function	Type
SDI/$\overline{\text{SDI}}$	3, 4	Non-inverting and Inverting Serial Data Input to the adaptive equalizer	CML input
$\overline{\text{SDO1}}$/SDO1	22, 23	Non-inverting and Inverting Differential Serial Data Output	CML output
$\overline{\text{SDO2}}$/SDO2	19, 20	Non-inverting and Inverting Differential Serial Data Output	CML output

Table 2-3. Control/Interface Pins

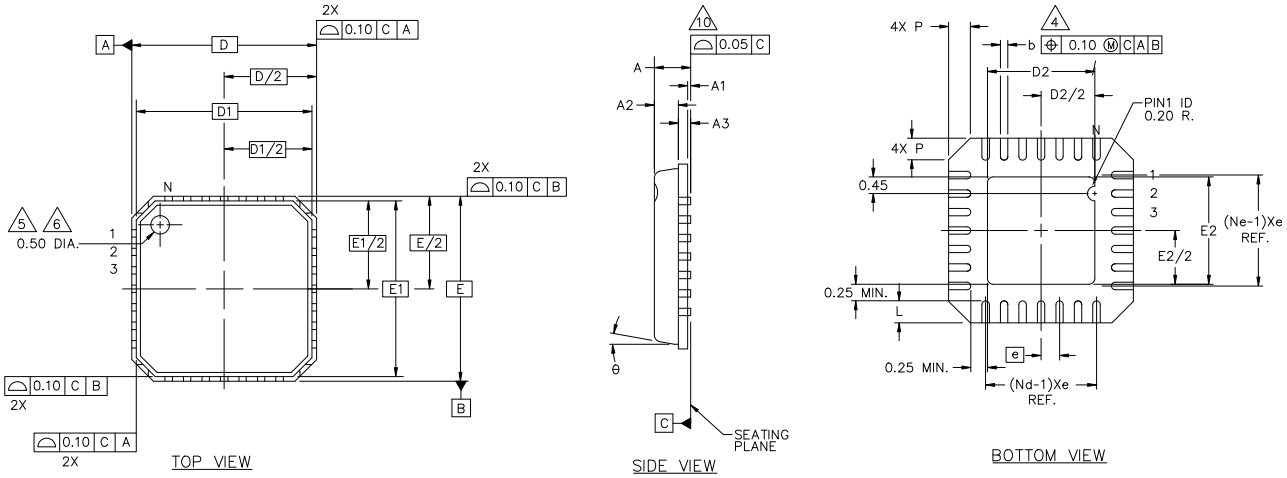
Pin Name	Pin Number	Function	Default	Type
NC	1	Do not connect.	N/A	N/A
SDO2_EN	5	Enable Input for **SDO2** Outputs: Low = SDO2 output disabled High = SDO2 output enabled	Internal pull down	CMOS input
SWING_L/H	6	Enable Input for High Swing Output on SDO1/2: Low = 750 mV_{PP} diff. (default) High = 1050 mV_{PP} diff.	Internal pull down	CMOS input
AGC/$\overline{\text{AGC}}$	9, 10	External AGC (Automatic Gain Control) capacitor connection points. Use 1.0 µF capacitor.	Internal pull up	Analog input
EQ_BYP	11	Input control signal that when enabled (High) bypasses the inputs directly to the output stage. Low = Normal operation High = Disables EQ and bypasses input to output	Internal pull down	CMOS input
NC	12, 13	Do not connect.	N/A	N/A
THRESH	14	Input control signal voltage. Programmable cable length forced mute threshold. This function is disabled if **LOS/MUTE** = Low	Internal pull down	Analog input
NC	15, 16, 17, 25	Do not connect.	N/A	N/A
LOS/MUTE	28	Bidirectional signal that can be used as an input control signal or as an output status indicator. When configured as an input by forcing a voltage on **LOS/MUTE** = High, the SDO outputs will be inhibited at logic low (outputs muted). See Table 1-4 for CMOS input levels. When **LOS/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled. When configured as an output (tied to a high-impedance input) or left floating, the programmable inhibit based on cable length is enabled. See Table 1-8 for **LOS/MUTE** pin output levels. Configured as Output: Low = Input signal detect High = Loss of signal Configured as Input: Low = Never mute High = Force Mute	—	CMOS input/ output
CLEN	29	Cable length Indicator output	—	Analog output
NC	31, 32	Do not connect to the pin.	N/A	N/A

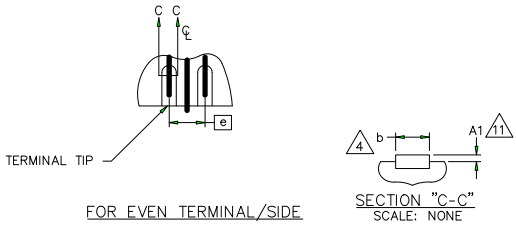
NOTE:
Internal pull-up/pull-down is 100 kΩ.

2.2 Package Drawing

The package for the M08046 is illustrated in Figure 2-2 below.

Figure 2-2. M08046 Packaging Details—Amkor





Note: View is for a 28 pin package. All dimensions in the tables apply for the 32 pin package

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	3.15	3.30	3.45	
E2	3.15	3.30	3.45	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

Please see Amkor's Application Note for PCB footprint (referenced in the Section A.2.1).

2.3 Manufactureability

The values shown in this section may change; however, these are standard requirements.

2.3.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000 V of ESD Human Body Model (HBM) testing.
Tested per JESD22-C101. This device passes 500 V of ESD Charged Device Model (CDM) testing.
Tested per EIA/JESD78. This device passes 150 mA of trigger current at 85 °C during Latchup testing.

2.3.2 Peak Reflow Temperature

M08046G (RoHS compliant package): Peak reflow temperature is 260 °C per JEDEC standards.

2.3.3 Moisture Sensitivity Level (MSL)

All versions of this device (Std Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

3.0 Functional Description

3.1 Pin Descriptions

3.1.1 General Nomenclature

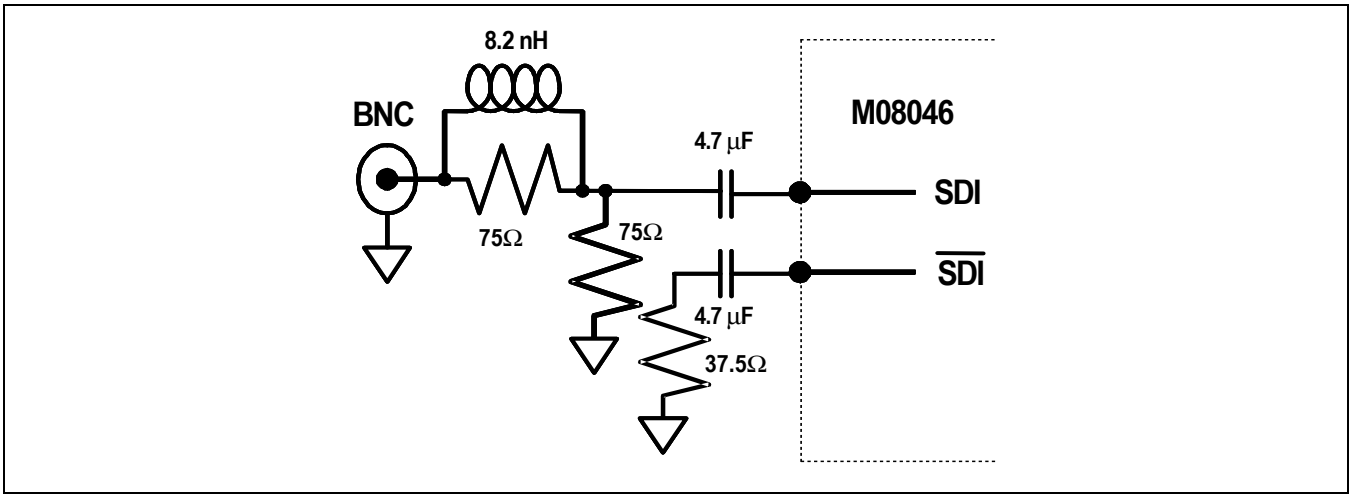
Throughout this data sheet, physical pins will be denoted in **BOLD** print. An array of pins can be called by each individual pin name (e.g. **MF0, MF1, MF2, MF3**, and **MF6**) or as an array (e.g. **MF[3...0, 6]** or **MF[3:0, 6]**).

3.1.2 High-Speed Input

Digital video coaxial cables are AC-coupled to the high-speed low-noise inputs **SDI/$\overline{\text{SDI}}$**, which are designed to operate in both single-ended and differential modes. The typical application is single-ended into the non-inverting **SDI** input with the inverting **$\overline{\text{SDI}}$** input biased to match the bias on the input used.

The M08046 does not contain any internal input terminations and requires both external input termination as well as the matching circuit to improve input return loss. The package and IC design of the M08046 have been optimized for high-speed performance, allowing it to have typical return loss values of 13 dB at 3 GHz and 30 dB at 1.485 GHz, using the recommended external matching/termination network and commonly employed right-angle, through-hole, or vertical mount 75 Ω BNC connectors. For a non-inverting single-ended operation, the recommended input circuit is shown in Figure 3-1. For a differential operation, the matching/termination circuit on **SDI** should be duplicated on **$\overline{\text{SDI}}$**. The internal pull ups automatically bias **SDI/$\overline{\text{SDI}}$** for proper AC coupled operations.

Figure 3-1. Single-ended Typical Input Matching/Termination Network



3.1.3 High-Speed Outputs

The high-speed CML differential outputs after equalization are made available on the **SDO1, $\overline{\text{SDO1}}$, SDO2, $\overline{\text{SDO2}}$** pins. By default only the **SDO1/$\overline{\text{SDO1}}$** outputs are enabled, **SDO2/ $\overline{\text{SDO2}}$** are enabled when **SDO2_EN** = High. Two swing levels are available; 750 mV_{PP} and 1050 mV_{PP}, when **SWING_L/H** = High, the 1050 mV output mode is selected, when **SDO2_EN** = High, this affects both **SDO1** and **SDO2**.

3.1.4 Adaptive Equalization Selection

In a typical operation, the adaptive equalization is enabled with **EQ_BYP** = Low; however, with **EQ_BYP** = High, the adaptive equalization and DC restore circuit is bypassed and the input is fed directly to the output.

3.1.5 Cable Length Indicator

When adaptive equalization is enabled (EQ_BYP = Low), an analog voltage inversely proportional to the cable length is made available on **CLEN**. The same transfer function applies to all bit rates. When adaptive equalization is disabled (EQ_BYP = High), the **CLEN** voltage goes to its highest value (this indicates 0 m cable length). During an LOS (Loss Of input Signal) event, the voltage falls to its lowest value.

3.1.6 Output Mute and Signal Detect

LOS/MUTE is a bi-directional pin that acts as an LOS detect output or a MUTE input.

When a voltage is forced on the pin, **LOS/MUTE** is a MUTE input. With **LOS/MUTE** = High (V_{DD}), the outputs of the M08046 will be inhibited at logic low. When **LOS/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled.

When the pin is tied to a high impedance node or left floating, **LOS/MUTE** is an LOS indicator output. In the event of an LOS, the output is muted. The inhibit threshold is set with an analog voltage applied to the THRESH input pin. This threshold will depend on cable type (e.g. Belden 1694A or 8281). To achieve maximum cable length equalization, the THRESH pin should be left open. Decoupling capacitors should be used between the THRESH pin and GND.

3.1.7 Equalizer Detailed Description

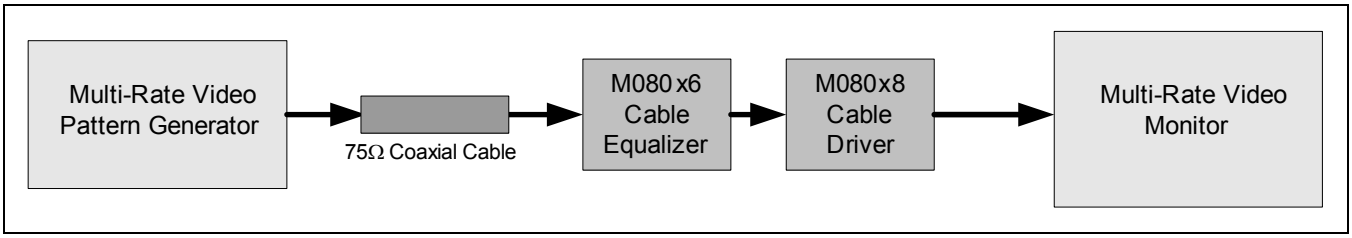
The basic equalizer design consists of interlaced stages of gain and equalization to maximize both the overall equalization gain as well as the input sensitivity for maximum performance with minimum jitter. In order to achieve maximum distance at 270 Mbps, 1485 Mbps and 2970 Mbps with Belden 1694A, the overall equalizer block has over 50 dB of broadband signal boost and maintains an input sensitivity of approximately 10 mV.

Since signals are launched with different rise and fall times which can vary substantially (especially at the receive end after going though a wide dynamic range of valid cable lengths) the equalization routine determines both the bit rate and the resultant signal HF attenuation as opposed to just looking at the launch edge rates. By determining both sets of conditions, it is possible to optimize the equalizer for the different rates. For example, the M08046 maintains the same maximum cable length as optimized SD-only equalizers. An SD signal through a short cable can have the same edge rate as an HD signal through a long cable; yet, both conditions require different levels of equalization as well as different optimized inverse-transfer functions. The advanced equalization technology can make the distinction between the two cases for optimal performance. This also leads to proper mute threshold (**THRESH**) and cable length indicator (**CLEN**) operation that is independent of the bit rate.

In order to accommodate both the worst case equalizer pathological patterns as well as some customer derived worst case DC offset patterns, a high-gain slicer is included in the signal path to correct for any eye-crossing

wander due to AC coupling of the input. Figure 3-2 shows the test set used by Mindspeed to evaluate the performance of the M08046.

Figure 3-2. Test Setup Diagram for Cable Equalizer Evaluation



Appendix

A.1 Glossary of Terms/Acronyms

BER	Bit Error Rate
CD	Cable Driver
CDA	Cable Distribution Amplifier
CML	Current Mode Logic
DDI	Differential Data Inputs
EMI	Electro Magnetic Interference
EQ	Equalizer or Equalization
ESD	Electro Static Discharge
GREEN	Environmentally friendly
HD	High Definition
HW	Hardware
ID	Identifier
I/O	Input/Output
QFN	Quad Flat No Lead
RoHS	Restriction of Hazardous Substances
SD	Standard Definition
SDI	Serial Digital Input
SDO	Serial Digital Output
SE	Single Ended
SW	Software

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- Application Notes for Surface Mount Assembly of Amkor's QuadFlatNoLead (QFN) Packages
- Amkor Technology Thermal Test Report TT-00-06 (See http://www.amkor.com for detailed information)

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